Design, Implementation, and Verification of a Data Acquisition System for the Prototypes of the Front-End Electronics of the $\bar{\text{P}}$ANDA Micro Vertex Detector

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***Abstract*—This paper describes the current status of the design, implementation, and test of a data acquisition (DAQ) system for the prototypes of the front-end electronics of the Antiproton Annihilation at Darmstadt ($\bar{\text{P}}$ANDA) Micro Vertex Detector (MVD). The features of this DAQ, called Juelich Digital Readout System (JDRS), are driven by the requirements imposed by the physics program of the experiment, such as continuous data collection without external triggering. Flexibility and modularity are thus key points for this system, which is meant to operate during a test beam, as well as in a laboratory environment. The implementation of the system is based on an off-the-shelf field-programmable gate array (FPGA) board. So far, two different application-specific integrated circuits (ASICs) have been successfully connected to the JDRS. Tests to establish the performance of the JDRS in terms of processing speed and reliability have been carried out and are still ongoing.**

I. Introduction

The $\bar{\text{P}}$ANDA experiment (Figure 1) will play a key role at the upcoming Facility for Antiproton and Ion Research (FAIR) in Darmstadt [1]. Exploiting proton-antiproton interactions, its scientific program addresses fundamental questions of Quantum Chromo Dynamics. The Micro Vertex Detector (MVD) is the sub-detector system closest to the interaction point (Figure 2) [2]. The primary task of the MVD is the reconstruction of the primary interaction vertex and the secondary vertices from the decays of short lived particles. The MVD consists of four barrel layers in the central part and six disk layers in the forward direction. It uses two different kinds of silicon detectors as sensitive elements: hybrid pixel detectors and double-sided microstrip detectors. Two different types of front-end application specific integrated circuits (ASICs) are thus under development for the MVD: the Torino Pixel ASIC (ToPix) and the $\bar{\text{P}}$ANDA Strip ASIC (PASTA). The ToPix ASIC is a chip developed for the readout of silicon pixel detectors. The final version of a single chip reads out more than 10,000 pixels with pixel dimensions of 100 µm x 100 µm. The PASTA chip is designed to read out silicon microstrip sensors. Like the ToPix ASIC, it measures the position, the deposited energy and the time of a hit. Both are designed to transmit untriggered data at a rate of hundreds of Mb/s to handle the expected hit rate in hot spots of the detector. A data aquisition system (DAQ) capable to handle these high rates is therefore needed. Such a system is called Jülich Digital Readout System (JDRS) and it is currently under development at the Forschungszentrum Jülich. The readout of the ToPix ASIC, which is now available in its fourth revision [3], has been succesfully integrated in the JDRS in the past [4]. Recently, some efforts have been made to adapt the existing system to the new ASIC prototype: the revision number one of PASTA [5], [6], [7]. Thanks to the modularity of the JDRS, a significant amount of both the software and the firmware can be reused without any modification.

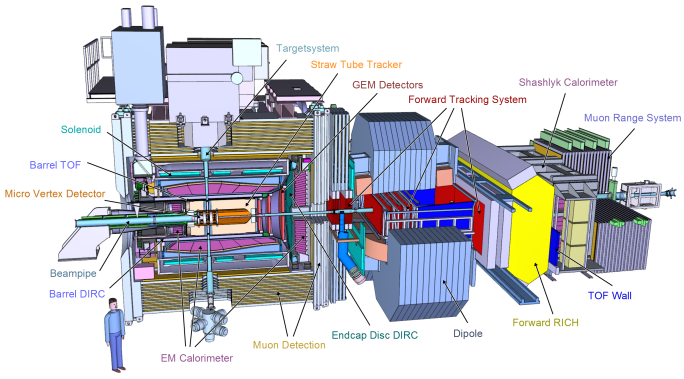

Fig. 1. The $\bar{\text{P}}$ANDA detector.

II. The $\bar{\text{P}}$ANDA strip ASIC: PASTA

PASTA is the 64 channel front-end chip, designed in a 110 nm CMOS technology to read out the strip sensors of the MVD. Its working principle is based on the Time of

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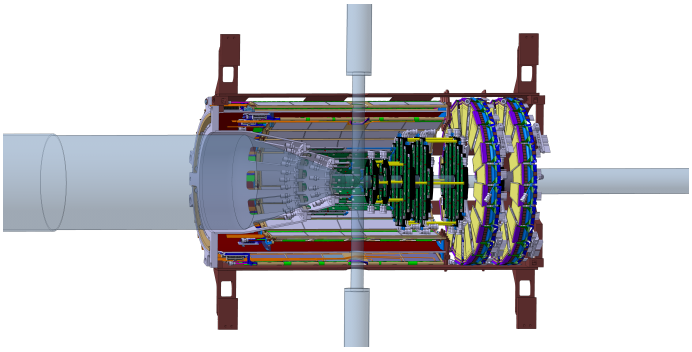

Fig. 2. A CAD drawing of the Micro Vertex Detector.

Flight for Positron Electron Tomography (TOFPET) ASIC, a chip intended for medical application to read out silicon photomultipliers [8]. PASTA delivers spacial, time, and charge information of the particles that hit the sensor, by means of the time over threshold (ToT) technique, based on two leading edge discriminators (Figure 3). The first discriminator has a lower threshold and it is used to resolve precisely the time of the leading edge of the signal. The correspondent branch takes the name of *time branch*. The second discriminator has a higher threshold and it is used to resolve the falling edge of the signal, in order to have an amplitude (i.e., deposited charge) information. The corrispondent branch is thus called *energy branch*. The higher threshold for the second discriminator is due the fact that the falling edge is slower than the rising one and therefore more susceptible to noise fluctuations, which would increase the signal jitter. A coarse and a fine time information are associated to each measurement. The resolution of the first one depends on the frequency of operation (clock resolution). The nominal value is 160 MHz, leading to 6.25 ns time resolution. The resolution of the latter is enhanced by means of a time interpolation, which leads to the nominal value of 50 ps. PASTA, differently than its predecessor TOFPET, will operate in a radiation intense environment. Therefore, specific protection measures have been implemented in the design. The main design specifications of the ASIC are summarized in Table I.

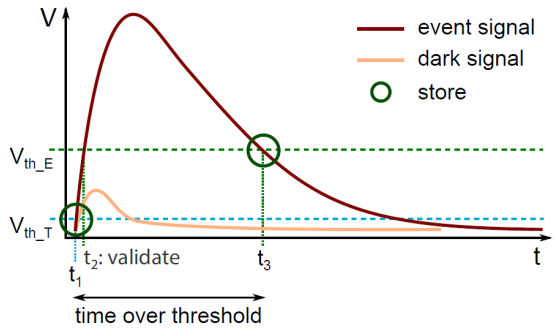

Fig. 3. ToT measurement in PASTA: based on two leading-edge discriminators [9].

TABLE I
MAIN DESIGN SPECIFICATIONS OF PASTA.

Self trigger capability	
Input capacitance/charge	Si Strips: 50 pF / 38 fC
Power consumption	< 4 mW/ch
Channel pitch	63 µm
Radiation tolerance	100 kGy
Efficiency gap	no evt loss
Charge resolution	8 bit dyn. range
Time resolution (coarse)	6.25 ns
Time resolution (fine)	$\sim$ 50 ps

III. THE JÜLICH DIGITAL READOUT SYSTEM

The JDRS has to be flexible in order to operate with different kinds of front-end electronics and easy to adapt to new prototypes. The main components of the JDRS are an evaluation board from Xilinx (ML605), hosting a Virtex-6 FPGA, and a custom-made readout board that hosts the device under test (DUT), i.e., the ASIC. A network link allows the connection from the evaluation board to a PC. The logic scheme for the FPGA, called firmware, is written in VHDL (Very High Speed Integrated Circuit Hardware Description Language). A software called MVD readout framework (MRF), based on C++, has been developed with the idea of maximum modularity in mind [10]. It is a library that collects functions which allow access to the elements of the readout chain. To facilitate this process, a Qt-based graphical user interface (GUI) has been developed. A schematic view of the system is shown in Figure 4.

IV. INTEGRATION OF PASTA WITH JDRS

A. Data Flow

Inside PASTA, the data corresponding to events that occurred in a specified time window are stored in a frame. Each frame is composed of a header, which contains information on the number of events, the data relative to the events (essentially coarse and fine time, and channel number), and a trailer, which contains a CRC (cyclic redundancy check) code to verify correct transmission. Since the ASIC operation is not based on a trigger signal, data is constantly sent over the transmission line. If no events occur, a frame with only header and trailer will be transmitted. The transmitted data is 8b/10b encoded to ensure a balanced line [11]. The data generated in the ASIC is then sent to the FPGA, where it is 10b/8b decoded and stored into a first-in-first-out (FIFO) buffer. The data from the FIFO can then be requested via

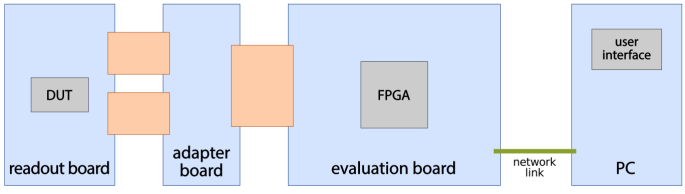

Fig. 4. Schematic view of the main components of the JDRS [9].

software and converted into a user-defined format (e.g., ASCII or Boost serializer). In order to obtain usable objects for the analysis of the performance, the data stream goes through another online decoding procedure, before being stored to disk. The visualization of the data is carried out using the *THttpServer* from ROOT [12].
The GUI widget responsible for the communication with the FPGA module, which receives data from the ASIC, and for the data handling is shown in Figure 5. In Figure 6, a screenshot of the *THttpServer* online monitoring is shown.

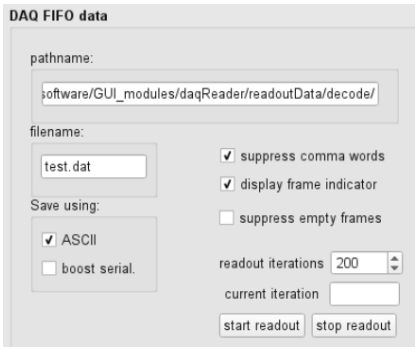

Fig. 5. GUI widget for data handling preferences.

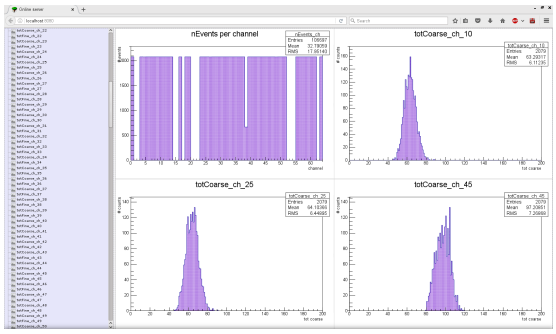

Fig. 6. A screenshot of the THttpServer online monitoring.

B. Configuration Optimization

PASTA has 46 global and 64-times 22 local configurable parameters that require optimization. A default configuration is loaded when the ASIC is powered on. Nevertheless, it is necessary to be able to access and edit this configuration from the user interface. Dedicated modules are implemented to send and read back a global configuration (i.e., sent to all the channels) and a local configuration (i.e., sent on a channel by channel basis).
PASTA has the possibility to generate a configurable test pulse, to mimic a sensor signal. A section of the JDRS is therefore dedicated to handle the configuration of such a test pulse. With this module, the user can specify parameters such as pulse length, width, and number of consecutive pulses. The test pulse can be used to study the performance of the chip in a laboratory environment and to optimize the configuration parameters. To facilitate this task, an automatic scanning procedure is available. In Figure 7, one can see the GUI widget corresponding to this module. Here the user can choose what kind of test pulse will be produced (i.e., a digital or an analog signal), which range of channels will be enabled, and up to two configuration parameters to sweep within a defined range. Once the measurement starts, the selected channels are enabled sequentially. For each of these, a train of pulses with parameters specified in the dedicated widget, is injected. When a satisfactory configuration is found, it can be stored to disk to be subsequently retrieved and loaded into the chip.

Fig. 7. GUI widget to automatize the procedure to test the chip.

V. Performance Measurements

The performance of PASTA is currently under evaluation. The aim is to proof the working principle and verify if the design specifications are met.
In the following discussion, the reader should keep in mind that the operating frequency has been limited to 80 MHz because the ASIC shows criticalities for clock frequencies above this value.

A. Laboratory Environment

Before operating the ASIC under an ionizing particle beam, it is useful to characterize its behavior in a laboratory environment, with radioactive sources and therefore lower data rate.
An important calibration that needs to be carried out, is the determination of the proper threshold value. If an incoming signal has an amplitude larger than the set threshold value, then such signal should be detected. Therefore, given a fixed pulse amplitude, it is reasonable to expect a progressive reduction of the number of detected events, with the increasing of the threshold value. The result in terms of number of events as a function of the threshold, for a given pulse amplitude, should look like an S-shaped curve, as shown in Figure 8. The suitable threshold for the given pulse amplitude is then the one that corrisponds to the detection of 50 % of the generated events. An alternative strategy for the threshold determination is basically the opposite of the mentioned threshold scan, for fixed pulse amplitude. It works, in fact, fixing the threshold and varying the pulse amplitude in the allowed interval.
In the case of PASTA the determination of the threshold by mean of the S-curve is not ideal. In fact, in a pulse amplitude scan, given a threshold, we observe that the number of detected events corresponding to the smallest generated amplitude is almost zero. While for the nearest bigger generated amplitude,

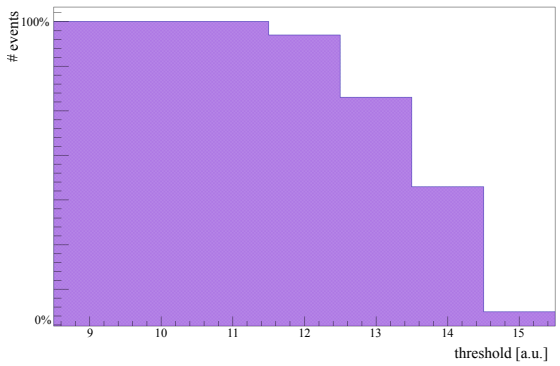

Fig. 8. Classic S-curve shape of the plot of the number of detected events as a function of the threshold value, for a fixed pulse amplitude.

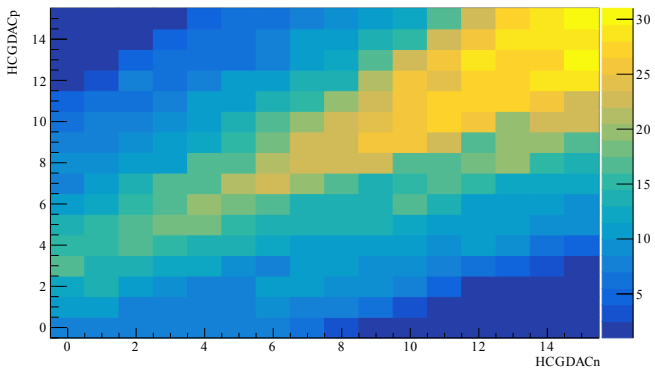

Fig. 9. Valid combination of the threshold parameters. The color code shows the number of channels for which the combination is valid.

the number of detected events is already 100 %. This means that even the smallest step between two consecutive amplitudes is still too big to allow to see a smooth transition and identify the threshold value as described above. Moreover, PASTA has two parameters, instead of one, to define the global threshold: HCGDACp and HCGDACn. The difference of these two (HCGDACp−HCGDACn) defines the threshold as the midvalue of an interval with predefined amplitude. Therefore, to analyze the behavior of the chip as a function of the threshold, we have to study a two dimensional information given by the combination of the two threshold parameters.

The strategy that we use to determine the threshold is the following: given a pulse amplitude, we inject a defined amount of pulses on each channel, repeating for every possible combination of the threshold parameters. We tag as valid the combinations of HCGDACp and HCGDACn that correspond to a number of detected events between 50 % and 110 % of the generated ones. We take as global threshold the combination that is valid for the majority of the channels.

The result of this measurement, for a pulse amplitude corresponding to 2 fC, is shown in Figure 9. Although all the combinations are shown, we consider only the ones where HCGDACp $\geq$ HCGDACn. Such a condition is imposed by the design of the circuitry and it is backed up by simulations.

The combination that is valid for the majority of the channels is HCGDACp = HCGDACn = 15 which corresponds to the minimum threshold achievable. It is, nevertheless, suitable only for roughly half of the channels of the whole ASIC. Among the rest of the channels, some are completely unresponsive, some show a high noise level, and some others are properly functional, but for different global threshold settings. PASTA offers the possibility to fine tune the thresholds on a channel by channel basis by using local threshold parameters. In this way a few other channels can be brought into operating conditions. The threshold determinations appears less critical for signals with bigger amplitude. Following, an example of the chip response for an injected pulse corresponding to 20 fC and optimized parameters for such amplitude (Figure 10). One hundred pulses, of 20 fC each, are injected into all the channels in a sequential scheme (from channel 0 to channel 63). Almost all the channels correctly detect the total number of generated pulses. Only a few of them do not respond to the stimuli at all, or only partially. The same measurement performed on other PASTA ASICs shows consistent results, although the pattern of malfunctioning channels might be different. At present, the cause for such behavior is still under investigation.

PASTA has been designed to have a working range that spans

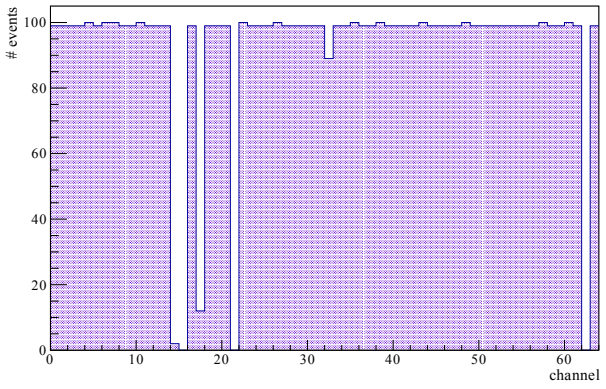

Fig. 10. Channel response for one hundred injections, each of 20 fC.

deposited charge from rather small values (around 1 fC) up to 40 fC. Within this range, the time over threshold as a function of the deposited charge is expected, by design, to show a linear behavior. To verify that, for each integer charge in the range, we generate one hundred pulses and we calculate the mean value of the ToT sample. The injection is performed sequentially, from channel 0 to 63. Figure 11 shows the result of such measurement for a single channel, which confirms the expected linear behavior.

B. Beam Test

PASTA has been recently tested under a proton beam at COSY (Forschungszentrum Juelich - Germany). Although a detailed analysis of the collected data is still ongoing, here we present some first results.

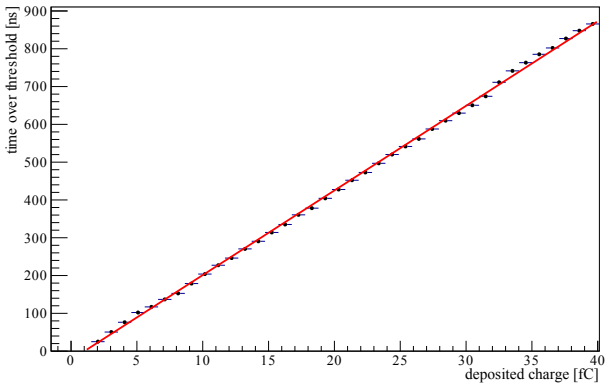

Fig. 11. Linearity of the ToT as a function of the deposited charge.

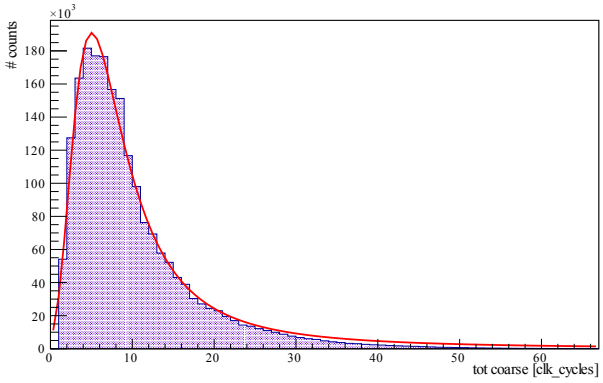

Fig. 13. Cumulative time over threshold distrubution: Landau shaped as expected.

In Figure 12, one can see the chip response for a beam momentum of $800\,\mathrm{MeV}\,c^{-1}$. Some among the channels that appear unresponsive have been disabled, due to a too high noise component. The rest does not respond to the stimuli in the used configuration. In Figure 13 we show the cumulative ToT distribution using the coarse time information (i.e., clock resolution), which shows a Landau shape as expected. Information on the fine timestamp resolution is not available at this stage of the data analysis.

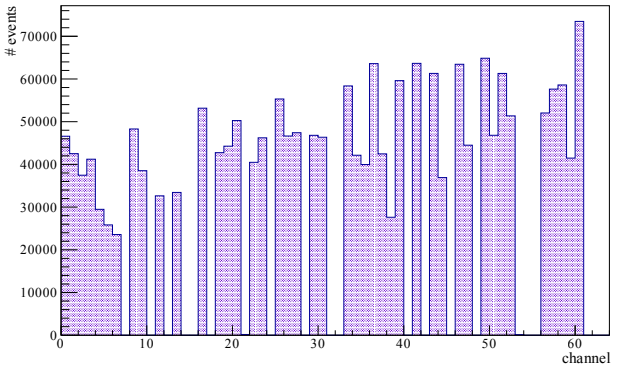

Fig. 12. Response of the chip under proton beam with $800\,\mathrm{MeV}\,c^{-1}$ momentum.

VI. Conclusion

A data acquisition system for the ASIC prototype of the PANDA MVD is under development at Forschungszentrum Juelich, Germany. The aim is to have a unique testing tool for the different prototypes of pixel and strip front-end chips. Here we showed the main features of such a readout system and the validation of its functioning when connected to the first revision of the strip front-end ASIC PASTA.

Tests with low interaction rates and under a proton beam allowed to prove that the basic measurement principle works as expected. Nevertheless, some critical issues have been observed, e.g., the thresholds determination for small deposited charge and some malfunctioning channels.

A new ASIC for the readout of the strip sensors of the MVD is under study and therefore a thorough investigation of the performance and weak points of PASTA is mandatory. It is foreseen to proceed in the future with a dedicated measurement campaign using radioactive sources as well as particle beams.

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