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Towards the integration of the Micro Vertex Detector in the $\overline{\text{P}}$ANDA experiment

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The $\overline{\text{P}}$ANDA experiment will make use of cooled antiproton beams of unprecedented quality that will be available at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt. It includes the Micro Vertex Detector (MVD) as innermost detector of the traking system, specially able to detect secondary vertices of short-live particles. Due to the forward boost the MVD layout is asymmetric with four barrels surrounding the interaction point and six disks in the forward direction. The innermost layers are composed of hybrid epitaxial silicon pixels and the outermost ones of double-sided silicon strips, with 10.3 x 10^6 pixels and 162 x 10^3 strip channels. $\overline{\text{P}}$ANDA features a triggerless architecture, therefore the MVD has to run with a continous data transmission at a high interaction rate (10^7 interaction/s) where hits have precise timestamps (the experiment clock is 160 MHz). In addition the energy loss of particles in the sensor should be measured. To cope with these requirements custom readout chips are under development for both pixel ans strip devices. The powering and cooling are challenging since the MVD volume is limited by the surrounding detectors and the routing is only foreseen in the backward direction. Support structures are made of carbon fibers and high thermally conductive carbon foam with embedded cooling pipes beneath the readout chips is integrated. The design of the MVD is an advanced stage and its technological aspects will be reported.

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1. Introduction

The $\overline{P}$ANDA experiment will be placed in one of the straight sectors of the High Energy Storage Ring (HESR) at the FAIR facility [1]. A reaction rate of about 2 x 10^7 s^{-1} is reached by the interactions between the nominal value of 10^{11} antiprotons, available in the 1.5÷15 GeV/c momentum range, and the internal target (pellet or cluster-jet type). The experiment will cover a wide range of physics topics [2]: spectroscopy of charmonium and of open charm mesons, search for gluonic exicitations, spectroscopy of charmed baryons and study of nucleon structure by measurements of time-like form factors, Drell-Yan and generalized parton distributions, modification of the properties of mesons embedded in nuclear medium and properties of double hypernuclei. The study of all these physics topics requires detectors able to identify pions, kaons, protons as well as electrons and muons in a large momentum range from about 200 MeV/c up to 10 GeVc. The reconstruction of short lived particles such as charmed mesons can be pursued with a vertex detector with a spatial resolution better than 100 μm. Photons from many physics channels demand an Electromagnetic Calorimeter (EMC) featuring low photon threshold, few MeV, and large dynamic range, up to 10 GeV. Exclusive measurements of the final states can be obtained with almost 4π coverage. Parallel physics topoligies can be operated on the same data sample using a self-triggering readout scheme where the frontend electronics digitizes and continuously transmits the data to a computer farm. The syncronization of the whole apparatus is obtained using a 160 MHz clock signal. $\overline{P}$ANDA is an internal fixed target experiment with an asymmetric layout around the interaction point to cope with the Lorentz boost. Particles emitted in antiproton–proton annihilations are concentrated in the forward acceptance of the detector, while in the antiproton–nucleus interactions the region close to polar angles of 90° corresponds to the highest occupancies. The setup of the experiment [3] consists of two systems: the Target Spectrometer (TS) and the Forward Spectrometer (FS). The TS is based on a 2 T superconducting solenoid housing the detectors in a onion shell like layout around the interaction point. The pipes for the pellet or jet targets cross the TS intersecting the beam pipe. The first detector surrounding this cross is the MVD.

2. Micro Vertex Detector

Primary vertex reconstruction and identification of secondary verteces displaced some hundred of micrometers from the primary one are the major tasks of the MVD. In addition the MVD improves the momentum resolution (in the order of one percent) adding its information to the whole tracking system and supports PID of low momentum particles by energy loss measurement.

Then good spatial resolution is requested: some tents of μm in the transverse plane and better than 100 μm along the antiproton beam direction. An accurate time-tagging of hits requires a time resolution in the order of some nanoseconds rms or better. The MVD [4] is designed to provide at least four hits per track while keeping a limited material budget (X/Xo less than 1 per each layer). It has to be able to manage a radiation fluence of about 10^{14} 1 MeV equivalent neutron/cm^2, estimated per 10 yers (50 % duty cycle of data taking) for antiproton–proton interactions and 15 GeV/c antiproton beam momentum, in the meanwhile a total ionizing dose of less than 100 kGray is expected. It will work at room temperature, in order to simplify the layout, which foresees routing and services only in the backward region. Four cylindrical layers arranged around the interaction

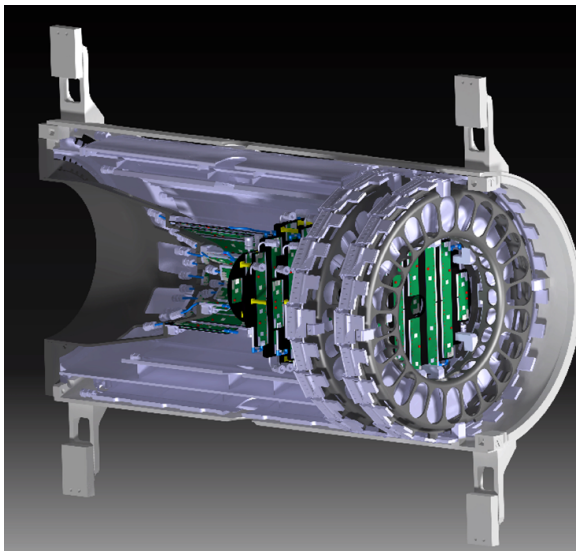

Figure 1: Vertical section of the barrel part and disks. The pixel modules are in green, the strip sensors and their readout in gray

point and six disks in the forward direction define the asymmetric layout of the MVD, 46 cm lenght and extended up to a maximum radius of 13.5 cm, covering the $3^\circ \div 150^\circ$ angle range. To manage higher rates the innermost layers as well the disks are composed of silicon pixel detectors with a total active area of 0.106 m^2. Double–sided silicon microstrip detectors equip the outermost layers and complete the two last disks at outer radius with a total active area of 0.494 m^2. The MVD is mechanically based on two halves suspended to the central tracker support and closed around the interaction region. The vertical section of the MVD barrels and the disks are shown in Fig. 1.

2.1 Pixels and Strips

The pixel detectors are based on the standard hybrid technology with a pixel cell size of 100 μm x 100 μm chosen according to the simulations. The sensor is a 100 μm n-epitaxial silicon layer featuring a resistivity of some kΩ cm grown on a Czochralsky (Cz) substrate with a lower resistivity (20–50 mΩ cm). The Cz substrate is thinned from 525 μm thickness down to 20 μm and it is the ohmic contact for the sensor biasing. The triggerless readout is foreseen to be an ASIC, bump bonded to the sensor, developed in 130 nm CMOS technology. The pixel module layout is based on a basic unit corresponding to a readout chip size and modules of several sizes are obtained by tiling from two to six units to obtain the best coverage of the disk part. In total 176 sensors house 810 readout chips. A pixel disk is composed of two half parts each built of pixel modules glued in an alternated configuration on both sides of a 4 mm carbon foam layer with embedded cooling pipes beneath the chip readouts. The two pixel barrels are composed of staggered staves each built of pixel modules glued on a 2 mm carbon foam layer supported by a carbon fiber structure featuring a Omega shape and housing the cooling pipe. First full size sensor prototypes were obtained with a 4 inch epitaxial silicon [4] wafer, used to test the thinning process of Cz substrate. Several radiation tests were performed using test structures to investigate the epitaxial material at different radiation levels with neutrons at the LENA laboratoty (Pavia) [4]. Tests of cooling of first

half-disk and stave prototypes using resistors as dummy chips have been done to define the final size and material of capillaries, the suitable glue and the cooling fluid. A power consumption of the readout electronics lower than 0.8W/cm^2 with an additional safety factor of 20% has been taken into account. Ni-Co chromium-molybdenum alloy capillaries (provided by Minitubes company) with a wall of 80 μm and 2 mm external diameter feature excellent corrosion resistance and good ductibility and toughness. These ones will be connected to flexible polyurethane pipes featuring higher diameter to reduce pressure drops and to allow a more easy operation of tube bending. Artic Alumina [4] glue allow good results, but it features rapide polimerization. However, the non uniformity in glueing operation and the presence of hot spots because of carbon foam structure have to be still correctly addressed. The strip part foresees three different geometries: square and rectangular sensors equip the two barrels and trapezoidal sensors compose the last two disks. The square sensor features 3.5 cm x 3.5 cm size and 512 x 512 strips with a 67.5 pitch and 90° stereo angle between p-side and n-side. The rectangular sensor features 6 cm x 3.5 cm size and 896 x 512 strips with a 67.5 pitch and 90° stereo angle. The trapezoidal sensor features 6 cm x 3.5 cm size and 768 x 768 strips with a 45 pitch and 15° stereo angle. All the strip sensors are 285 μm thick. The readout is every second strip. Full size sensor prototypes for all three geometry were produced by CiS company (Erfurt) using 4 inch float zone wafers. The strip support is a sandwich made of carbon fibers (M55J) and rohacell foam. This last material is substituted by carbon foam (POCO HTC) beneath the front end chips to increase the heat dissipation towards the embedded cooling pipe. The support features windows corresponding to the strip sensors to reduce the amount of material even if the the stiffness is garanteed. Both punch-trough and poly-Si biasing were tested, as well the electrical functionalities. Several tests were performed with particle beams at CERN and COSY [4].

3. Readout Architecture

The challenging request of a triggerless readout suggested to develop custom readout electronics for both pixel and strips. Meanwhile the GBTx [5], GBTIA, GBLD and Versatile Link projects [6] (below generically indicated as GBT), under development at CERN for the LHC upgrades, appeared the solution to be included in the readout chain for the electrical–optical conversion to reduce the electrical data transmission lines in favour of fast optical data links. In addition, the interface to the front-end electronics is managed via ten 320 Mb/s serial links based on the SLVS (Scalable Low Voltage Signaling) differential standard, in order to be compatible with the 1,2 V voltage supply typical of deep submicron technologies. The MVD Multiplexer Board (MMB) is the off-detector electronic based on Advanced Mezzanine Cards (AMC) for microTCA that will manage data from up to three GBTs for both pixel and strip parts and send them to the FPGA-based Compute Nodes of the $\overline{P}$ANDA DAQ sytem, using a 10 Gb/s optical link. In addition it receives the clock signal from the time distribution system (SODA) of the experiment. Both strip and pixel front-end chips will be biased using voltage regulators based on the radiation tolerant DC-DC converters [7] developed at CERN for the LHC upgrades and using air core inductors to be compatible with the magnetic field.

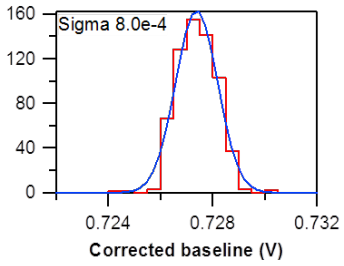

Figure 2: Corrected baseline distribution for 640 readout channel pixels of ToPix4

3.1 Pixel Readout Chain

The readout scheme of the pixel detector is based on the concept of module, a three layer structure: the ASICs, named ToPix, bump bonded to the sensor and wire bonded to the hybrid bus glued to the top of the sensor. The hybrid bus featuring a staircase section, routes both signals and power lines and it is connected to two service boards: the GBT circuit and the DC–DC voltage regulator fed by the power supply. An aluminum strip cable connects the hybrid bus to the GBT circuits and the data are trasmitted using the e–link, electrical port featuring 320 Mb/s. Currently the fourth readout generation prototype of a reduced scale ASIC has been produced and it is under test, a 640 pixel readout channel matrix out of 12760 of the final version. This chip was realized with a Multi Project Wafer in 130 nm CMOS technology and it contains all the relevant features: triggerless readout, charge encoding using the Time over Threshold Technique (ToT), double column readout, Hamming encoding and Triple Modular Redunancy (TMR) pixel logic protection to the Single Event Upset [8], leading and trailing edge registers with DICE protected latches, end of column buffering, Single Data Rate (SDR) and Double Data Rate (DDR) serial output and GBT compatible SLVS input/output. Preliminary results with a clock signal running at 160 MHz show a narrow corrected baseline distribution (Fig. 2) obtained with an easy calibration using 640 pixel DACs complitely linear. And the ToT linearity has been measured for the whole input range using a test pulse.

Using the third version of ToPix, the reduced scale ASIC was connected to a 100 μm epitaxial silicon sensor to produce first single-chip hybrid pixel assembly. The pixel matrix features 640 channels. Four assemblies were combined to obtain a pixel tracking station and a test was performed at CERN with a 10 GeV/c pion beam to study the operation of the triggerless readout [9]. During this test a 50 MHz clock signal was used. The pixel raw data include column and row numbers, leading and trailing edge information from the ToT measurement, the first one being the timestamp of the hit. For each assembly a timestamp ordering process is done and then a timestamp matching among all the assemblies is performed to assign the hits belonging to the same track to a common event. After the track reconstruction ToT distributions are obtained, which can be fitted with a convolution of Landau plus Gaussian distributions. A measured cluster size of 2.5 was evaluated at the 60° rotation angle between the assembly under study and the incident particle beam. An efficiency of 98% is reached at a threshold value of about 685 electrons for the same assembly. A hybrid bus prototype featuring a structure for six readout chips was produced at CERN according to the MVD design. It implement 4 direct differential pairs to each chip and 3 differential pairs in daisy chain, its size is 67.9 mm x 11.9 mm and the tracks featuring 60 μm width and 15

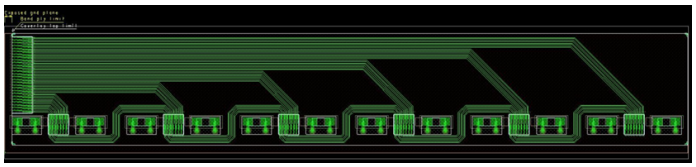

Figure 3: Layout of the hybrid bus prototype

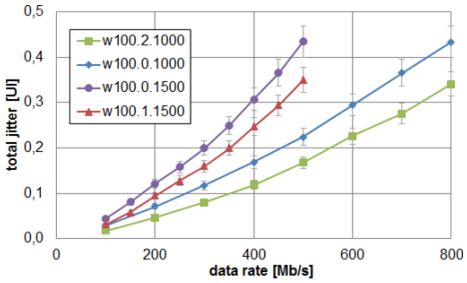

Figure 4: Total Jitter as a funtion of the data rate for four different cables. Green square, 1 m long cable, track uncovered; blue diamond, 1 m long cable, track covered; red triangle, 1.5 m long cable, track uncovered; violet circle, 1.5 m long cable, track covered

μm thick, 60 μm spacing, are made of aluminum glued on the top of a 75 μm thick kapton layer. A aluminum ground plane is positioned on the backside and a kapton cover garantees the tracks protection (a value of about 100 ohm differential impedance was obtained with the simulation of the prototype), 12 smd capacitors pads were included in the prototype. Fig. 3 shows the bus layout. A dedicated testing board allows the characterization of the direct pairs with SLVS signals from a Pattern Generator. SLVS signals driven by trasmitters up to 320 Mb/s feed the daisy chain pairs. The measured jitter values are acceptable for all the setups because at the 320 Mb/s data rate (e–link data rate) they are lower than 0.1 Unit Interval (UI) value (0.3 UI is the standard limit). The simulations show that the main component affecting the material budget of the MVD is the cabling (38%) [4]. For that reason the present MVD layout foresees interconnections between the ASICs and the GBTs made of aluminum instead of copper material in the active volume of the detector. Prototypes based on the laminated aluminum technology were designed at INFN Torino and manufactured at CERN. The layout foresees 18 differential pairs with tracks featuring 100 μm width, 15 μm thick and 100 μm spacing. A 75 μm thick kapton layer including glue is between the tracks and a 15 μm thick aluminum ground layer protected by a cover layer. Several prototypes featuring 1m and 1.5 m long differential pairs, with and without track covers have been carried out. Total jitter was measured with SLVS signals as a function of the data rate and in Fig. 4 four different prototypes are compared. At the data rate of the e–link all the prototypes show values lower than the standard limit of 0.3 UI. Then the hybrid bus protoype and a 1.5 m long cable were arranged togheter using a wire bonding connection. In this setup the measured total jitter corresponding to 320 Mb/s is lower than 0.2 UI.

3.2 Strip Readout Chain

The readout scheme [10] of the strip detector is based on the concept of module: a Module Data Concentrator ASIC (MDC) multiplexes data from all the ASICs, named PASTA (PANDA

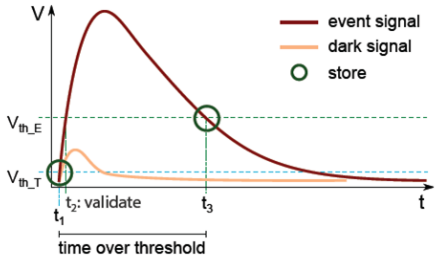

Figure 5: The double threshold method implemented in the PASTA chip.

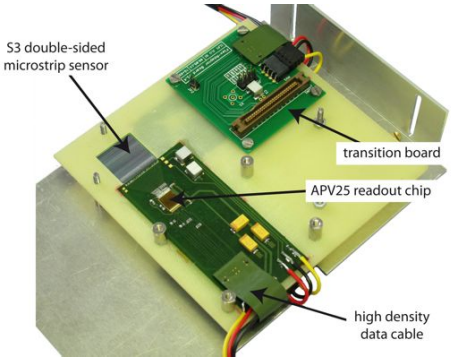

Figure 6: Full size square strip sensor and flex PCB

Strip Asic), connected to a strip sensor, an hybrid flexible PCB (flex PCB) houses the MDC and PASTA chips for many sensors and their signal and powering routing. This flex PCB is connected to the GBTs circuit and to the DC–DC converters as in the pixel scheme. PASTA is under design as a development of the TOFPET project [11] and the first full size layout will be submitted to a Multi Project Wafer run in 110 nm CMOS technology within the end of 2014 year. It is a self triggered chip featuring 64 channels with a channel pitch of 60 μm and 4.2 mm x 5 mm size. The requirements are: input capacitance lower than 50 fF, dynamic range lower than 50 fC, power consumption lower than 4 mW/ch, radiation protection in the order of 100 kGy, dynamic range of 8 bit. Its architecture foresees two thresholds applied to the amplified signal. The lower one gives the first time information to allow the ToT value and the hit time, the second one validates the hit and gives the second time information of ToT. In addition, a time interpolation method measures the time interval between the previous threshold crossing values and the clock signal edges. This technique allows time tagging in the order of 100 ps (Fig. 5). The flex PCB, folded around the strip stave, will connect p-side and n-side readouts to the MDCs. A first reduced scale prototype has been produced by GS Swiss PCB AG manufacturer using 12 μm thin copper layers and 50 μm thick intermidiate kapton foil with laser vias featuring diameter of some hundreds of μm, 15 μm thin varnish covers protect both sides. A full size (3.5 cm x 3.5 cm) square strip sensor was connected to the first flex PCB prototype and readout with APV25 chips (Fig. 6). This system was tested at COSY at the beginning of 2014 year with acceptable results.

4. MVD Service Integration

The service integration for the MVD project is very challenging. In fact all GBTs circuits and DC–DC converters have to be arranged around the beam pipe immediatly upstream the MVD in a cylindrical volume featuring the 30 cm external diameter of the detector, including routing and cooling pipes distribution. This layout is requested by the integration of the backward calorimeter that has a central hole featuring a 30 cm diameter. This detector will slide with its support along the beam pipe and the MVD services up to the final position, upstream the MVD. In particular 24 twin cooling bars equipped with 88 circuits each will house all the needed DC–DC converters. And 12 cooling bars equipped with 14 circuits each will arrange the needed GBTs. The thermal simulations of these equipped bars are in progress.

5. Conclusions

The MVD integration in the $\overline{P}$ANDA experiment is very challenging in particular for what concerns the services. To achieve the final project, custom developments have been studied and implemented as reported in the Technical Design Reports already written. Further developments for the readout of both pixel and strip are ongoing and detector protoypes have been assembled and tested to validate the design of each components and the triggerless readout.

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