Doctoral Thesis

Read-out and online processing for the Forward Tracker in HADES and $\overline{\text{P}}$ANDA

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Dedicated to my parents and beloved brother

Oświadczenie

Ja niżej podpisany Akshay Malige doktorant Wydziału Fizyki, Astronomii i Informatyki Stosowanej Uniwersytetu Jagiellońskiego oświadczam, że przedłożona przeze mnie rozprawa doktorska pt. "Read-out and online processing for Forward Tracker in HADES and $\overline{\text{P}}$ANDA" jest oryginalna i przedstawia wyniki badań wykonanych przeze mnie osobiście, pod kierunkiem prof. dr hab. Piotra Salabury. Pracę napisałem samodzielnie.

Oświadczam, że moja rozprawa doktorska została pracowana zgodnie z Ustawą o prawie autorskim i prawach pokrewnych z dnia 4 lutego 1994 r. (Dziennik Ustaw 1994 nr 24 poz. 83 wraz z pó źniejszymi zmianami).

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Kraków, dina .....

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Abstract

Nuclear Physics
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Doctor of Philosophy

Read-out and online processing for the Forward Tracker in HADES and $\overline{\text{P}}$ANDA

by Akshay Malige

Forward Tracker (FT) developed for the $\overline{\text{P}}$ANDA - HADES experiments, will be used for tracking and identification of charged particles in the forward regions by measuring the drift-time and the energy loss with the Time Over Threshold (TOT) method of the track. In the thesis, the methods required to achieve the energy and position resolution for the tracker are developed and evaluated in two stages. In the first stage, the detector and readout calibration methods are developed to endow uniform gain characteristics from a large number of detector channels. These methods are also used for the qualification of PASTTRECv3 ASIC ($\overline{\text{P}}$ANDA Straw Tube Tracker REadout Chip, Application Specific Integrated Circuit) developed for the FT. The obtained calibration parameters are validated by tracking the performance of prototypes of straw tubes under realistic beam conditions inside the HADES experiment and prototypes of the $\overline{\text{P}}$ANDA detectors.

In the second stage, a Data AcQuisition (DAQ) system performing online event selection, filtering and particle track reconstruction on FPGA-based hardware has been developed and evaluated in experiments using proton beams and cosmic rays. The application of online event processing in FT will accelerate event processing and introduce data reduction, which is one of the components of the DAQ system in the $\overline{\text{P}}$ANDA experiment.

The FT detector setup and the DAQ have been integrated for the HADES experiment and the successful operation of the detector in the full system run has confirmed the effectiveness of the developed methods.

Streszczenie

Fizyka Jądrowa
Instytut Fizyki im. Mariana Smoluchowskiego

Rozprawa doktorska

Odczyt i przetwarzanie online dla Forward Tracker w HADES i $\overline{\text{P}}$ANDA

by Akshay Malige

Detektor Forward Tracker (FT) opracowany dla eksperymentów PANDA – HADES, będzie używany do rekonstrukcji śladów przelotu oraz identyfikacji naładowanych cząstek w przednich rejonach poprzez pomiar czasu dryfu oraz straty energii metodą Time Over Threshold (TOT). W tej pracy, metody potrzebne do uzyskania rozdzielczości energetycznej i pozycyjnej detektora zostały opracowane i sprawdzone w dwóch krokach. W pierwszym kroku, metody kalibracji detektora oraz systemu odczytu zostały opracowane w celu uzyskania jednolitej charakterystyki wzmocnień dla dużej ilości kanałów. Te metody zostały również wykorzystane do kwalifikacji układów PASTTRECv3 ASIC (PANDA Straw Tube Tracker REadout Chip, Application Specific Integrated Circuit) opracowanego dla FT. Uzyskane parametry kalibracyjne zostały potwierdzone poprzez sprawność rekonstrukcji śladów z detektorów słomkowych w rzeczywistych warunkach eksperymentów z wiązką w eksperymencie HADES oraz na prototypach detektora PANDA.

W drugim kroku, system akwizycji danych (Data AcQuisition system DAQ) wraz z selekcją zdarzeń, filtracją oraz rekonstrukcją śladów przelotu cząstek w czasie rzeczywistym na układach FPGA został opracowany oraz sprawdzony w eksperymentach z wiązką protonową oraz promieniowaniem kosmicznym. Zastosowanie przetwarzania zdarzeń w czasie rzeczywistym dla FT przyspieszy przetwarzanie danych oraz wprowadzi redukcję ilości danych, co jest częścią systemu DAQ w eksperymencie PANDA.

Systemy detektorów FT oraz DAQ zostały zintegrowane z eksperymentem HADES a pomyślne działanie detektora w pełnym systemie potwierdziło skuteczność opracowanych rozwiązań.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, prof. hab. Piotr Salabura, for the guidance, support, and encouragement throughout my PhD journey. He has been a constant source of motivation and has always challenged me to think critically and push the boundaries of my research. I feel truly fortunate to have had the opportunity to work with such an exceptional mentor.

I would also like to express my sincere gratitude to my co-supervisor, dr Grzegorz Korcyl, for his invaluable contributions to this journey. His expertise, support, guidance and friendship have not only been instrumental in shaping the direction and quality of my work, but also my personality. He has been an inspiration in many forms and I am grateful to him.

I would like to extend my thanks to other members of the HADES-PANDA experiment, with particular emphasis on the Cracow group: prof. Jerzy Smyrski, dr hab. Witold Przygoda, dr Rafał Lalik, dr Izabela Ciepał, dr Narendra Rathod, dr Krzysztof Nowakowski and mgr Konrad Sumara. I would also like to thank all my colleagues from the cluster of nuclear physics departments. They were always kind to me and supported me.

I would also like to thank the members of my dissertation committee, for their valuable feedback and encouragement throughout the process.

I would like to express my deepest gratitude to my parents: Harish Malige and Usha Malige for their unwavering support and encouragement throughout my PhD journey.

Finally, I would like to thank my friends: Shivani, Arshiya Anees Ahmed, Sahil Upadhyaya, Subash Moolya, Bhargav V Bhat and Rajesh Acharya for their love, support, and understanding during this challenging but rewarding journey.

Collaboration Contribution statement

The studies described in the following thesis were conducted within the scope of the HADES and $\overline{\text{P}}$ANDA collaborations. Research done in collaboration implies a high level of cooperation between scientists and a splitting of duties. The main results of my work are presented in Chapters 3, 4 and 5. My contributions are described in detail below.

In the context of Chapter 3, the PASTTREC ASIC circuit was developed by the HADES - $\overline{\text{P}}$ANDA working group at the AGH University of Sciences, Kraków. The hardware, firmware and software for the TRB were developed by the TRB collaboration consisting of HADES members from GSI-Jagiellonian University and Technical University in Munich. The HADES - $\overline{\text{P}}$ANDA working group at UJ, Kraków, of which I am a member, contributed to the conceptual design of the ASIC, performed various tests with beams and radioactive sources and developed the software tools for the qualification of the PASTTRECs. To arrive at the results presented in this chapter, I constructed the test setup described in this chapter, executed the tests and measurements, created the analytical software tools, and carried out the data analysis.

In the instance of the results presented in Chapter 4, the construction of the FT prototype detector setup and the organisation of the beam time for the tests was a joint effort by the HADES - $\overline{\text{P}}$ANDA working group at UJ, Kraków and at Forschungszentrum Jülich. I prepared the configuration for the PASTTRECs and performed the tests of the readout before taking part in the data-taking during the test beam-time. I also developed the software tools, the data acquisition and analysis, which includes the track reconstruction algorithm to produce all the findings detailed in this chapter. I was later involved in the installation of the FT in the HADES experiment, setting up the readout and developing the control and monitoring tools required for FT during the data-taking experiment. The luminosity calculations from the collected data were performed by the HADES physics analysis group.

The data transmission architecture (GTH+network stack) of the data processing pipeline described in Chapter 5 was carried over from earlier works. The remaining parts, mainly the pipeline's first-stage filter, second-stage filter, tracking engine, and other auxiliary parts were developed by myself. To arrive at the results, I also built the setup and the tools necessary for developing, testing and optimizing the pipeline in simulations, laboratory tests, and beam emulations.

During my studies, as an active member of the HADES and $\overline{\text{P}}$ANDA collaboration, I took part in three experiments which took place in GSI Darmstadt and one test experiment which took place in Forschungszentrum Jülich. I have presented

my work at six collaboration meetings. Moreover, my results were presented on behalf of the HADES and $\overline{\text{P}}$ANDA collaborations during two conferences: MESON 2018 and FAIRness 2019 and published in IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 69(7) 17765-1772.

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List of Abbreviations

ADC Analog to Digital Converters

ASIC Application Specific Integrated Circuit

BLH BaseLine Holder

CLB Configurable Logic Block

CR Collector Ring

CTS Central Trigger System

CSP Charge Sensitive Pre-amplifier

DAC Digital to Analog Converter

DAQ Data Acquisition

DC Data Concentrator

EB Event Builder

ESR Experimental Storage Ring

FAIR Facility for Antiproton and Ion Research

FEB Front end Electronic Board

FEE Front-End Electronics

FPGA Field Programmable Gate Array

FRS FRagment Separator

FS Forward Spectrometer

FT Forward Tracker

HADES The High-Acceptance DiElectron Spectrometer

HESR High Energy Storage Ring

HL High Luminosity

HLS High-Level Synthesis

HLD HADES List mode Data

HR High Resolution

IC Integrated Circuit

LED Leading Edge Discriminator

LVDS Low Voltage Differential Signaling

MIP Minimum ionising particle

OPN Online Processing Node

PASTTREC $\overline{\text{P}}$ANDA Straw Tube Tracker REadout Chip

PLD Programmable Logic Devices

PZC Pole Zero Cancellation

RESR Recuperated Experimental Storage Ring

SPI Serial Peripheral Interface

STS Straw-tube Tracking Station

SODA Synchronization of Data Acquisition

TS Target Spectrometer

TRB Trigger Readout Board

TDC Time to Digital Converter

TDL Tapped Delay Line

TOT Time Over Threshold

UNILAC UNIversal Linear ACcelerator

Chapter 1

Introduction

Advances in particle physics account for a large portion of the underlying body of knowledge required to run many systems in our complex world. There is no equipment ordering catalogue available when physicists begin to measure novel physics phenomena. Many of the technologies have to be developed by themselves. Hence developed technology and equipment benefit the world in numerous ways. For example, the touch-screen technology developed at CERN has now become a standard interface for many devices. Another example is the World Wide Web, which was initially created to make it easier for people all over the world to communicate discoveries from particle physics. The Web has developed to a point that it currently generates trillions of dollars in yearly commercial traffic since its creation nearly 30 years ago. The value of tools and techniques developed extends far beyond particle physics to other areas of science and society.

One aspect of particle physics that sets it apart from all other sciences: it involves interactions of three forces – the strong, electromagnetic, and weak. Since Becquerel's discovery of radioactivity in 1896, the study of particle physics has been a continuing source of surprises, unexpected events, and novel insights into the laws of nature. The technical advancements of the 1950s made it possible to create high-energy particle beams in a laboratory. One new particle after another has been found during the past 50 years, primarily as a result of these laboratory experiments. The invention of high-energy accelerators, which could produce powerful, precisely regulated beams of known energy, was what would ultimately reveal the quark substructure of matter. The model that particle physicists now use to describe roughly 200 fundamental particles and their interactions is known as the Standard Model. With the help of six quarks, six leptons, and force-carrying particles, this model is incredibly successful in explaining all known particles as shown in Figure 1.1. Except for gravity-related events, this tries to describe all particle physics phenomena in terms of the characteristics and interactions of a limited number of elementary (or fundamental) particles, which are currently characterized as being point-like, devoid of internal structure or excited states. To comprehend the biggest mysteries such as what the cosmos is comprised of, what keeps it together and the events that took place during the universe's early history soon after the Big Bang, many mysteries at the subatomic levels must be understood by studying the interactions of particles at high energies.

For example, one of the greatest intellectual challenges of modern physics is to understand confinement not just as a phenomenon but to comprehend it quantita-

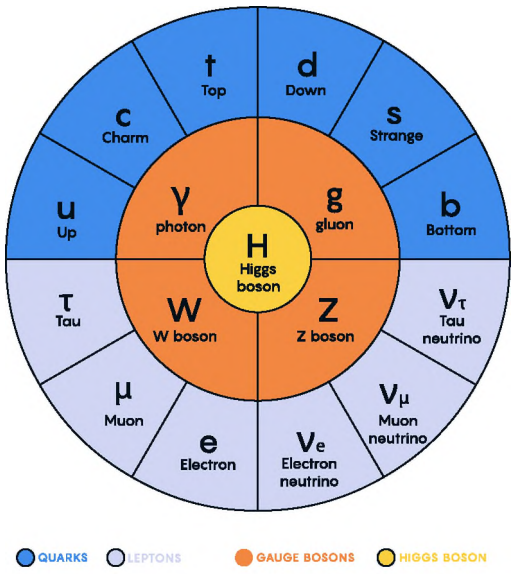


Figure 1.1: Schematic drawing of the fundamental particles of the Standard Model and their families.

tively from the theory of the strong force. Nucleons, which are made up of protons and neutrons, are a subclass of hadrons. They are made of quarks and connected by the strong force, which uses gluons as a medium. The force, which operates between two quarks, behaves in an unexpected way. When the quarks are close together, it is extremely tiny, expand as the distance widens, and then stay constant even when the quarks are separated from one another at ever-greater distances. When a quark-antiquark pair is split apart, the gluon field's energy increases until a new quark-antiquark pair may be produced. As a result, one obtains new quark-antiquark pairs rather than two isolated quarks. Another example is the puzzle of hadron physics that addresses the origin of the hadron masses, i.e. of the particles composed of quarks. In the nucleon, less than 2% of the mass can be accounted for by the three valence quarks. The production of new particles, new states and the investigation of the detailed structure of subatomic systems can be done using particle accelerators. High energies are crucial for creating novel states as well as learning more about the specifics of the structure of subatomic systems. It is clear that when the dimension under consideration shrinks, the particle energy must increase.

Over the past few decades, there has been a significant transition in both the programs and infrastructure supporting particle physics research. Through the 1980s, small accelerator facilities were the norm; but, larger, more potent facilities have started to take their place. The shift to major regional facilities was well underway at the start of the new century. The Facility for Antiproton and Ion Research (FAIR) at Darmstadt, Germany is one such experimental initiative set to explore broad areas of particle physics using relativistic heavy ion collisions. The LHC (Large Hadron Collision, CERN, Geneva) and RHIC (Brookhaven) high-energy collider experiments concentrate on the area of high temperatures and low net-baryon densities. Meanwhile, high net-baryon density areas are studied in fixed-target experiments like those at FAIR (see Figure 1.2). We need to build sophisticated and advanced detecting devices that can record particles produced in such high-energy

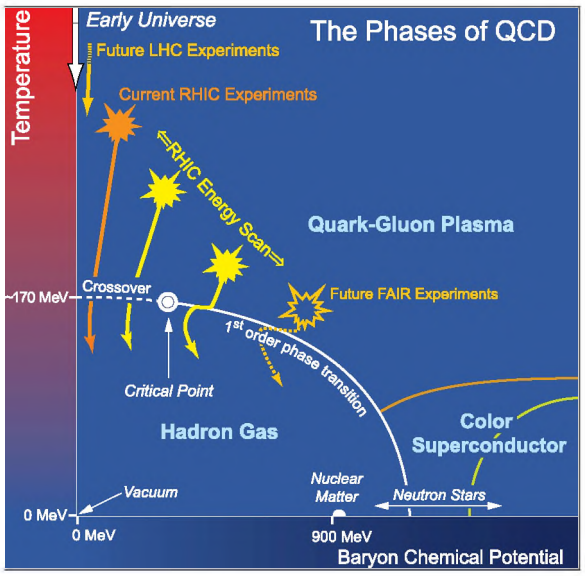


Figure 1.2: Schematic QCD phase diagram for nuclear matter. The solid lines show the phase boundaries for the indicated phases The solid circle depicts the critical point. Possible trajectories for systems created in the QGP phase at different accelerator facilities including FAIR are shown [1].

collisions to compare standard model predictions with the underlying physical properties of nature. Forward Tracker (FT) is one such sophisticated detector built for measuring charged particle momenta based on their trajectories in the HADES and $\overline{\text{P}}$ANDA experiments at FAIR. The main components of this measurement are the energy and the position of the particles passing through the detector. One of the main focuses of the work described in this thesis is to develop the methods required to achieve the energy and position resolution for this tracking detector in these experiments. To achieve this, the following goals must be met:

- Obtain the calibration parameters for the detector and the read-out to meet the design requirements of the detector in the $\overline{\text{P}}$ANDA experiment.
- Presentation of methods to improve the signal-to-noise ratio and subsequently enhance the lifetime of the detector.
- Presentation of a methodology for the qualification of FT front-end electronics.
- Installation of the FT at the HADES experiment and present the read-out configurations to measure p + p collisions at 4.5 GeV.
- The finalization of the components of read-out and operational parameters for the $\overline{\text{P}}$ANDA Forward Tracker.

In order to fulfil the above goals the following tasks had to be completed:

- Development of the tools and analysis methods to reconstruct particle tracks in the FT.
- Building a prototype detector and read-out and testing its tracking performance with different read-out and detector configurations under proton beams.

- Development of the tools and analysis methods to achieve uniform gain characteristics for a large number of detector channels and qualification of a large number of front-end electronics.
- Test the individual hardware components of the read-out and develop control software and firmware for the system.

The Data Acquisition system (DAQ) is the component of an experiment responsible for transporting the data from the detector read-out to the storage. Large-scale physics experiments running at high interaction rates place a high demand on the DAQ system. For this reason, the DAQ is typically designed so that only the particle interactions relevant to the experiment are selected and sent to storage (e.g. HADES). However, such selection is not feasible in experiments operating at high beam-target interaction rates, wide range of event topologies and a specific set of features. This makes it difficult to separate and identify interesting physics processes. $\overline{\text{P}}$ANDA is one such experiment operating at interaction rates up to 20 MHz [2] and will not use fixed event selection methods in the DAQ. As a result, data collection generates a large and continuous data stream of about 200 GB/s [3]. For example, the Forward Tracker (FT) can output between 1 GB/s and 10 GB/s [4] during active data taking. Even when no hits are registered by some detectors, the continuous read-out generates significant amount of data, limiting the flexibility of measurements. For this reason, an event selection method has to be designed based on real-time feature extraction, filtering, and high-level correlations in the early stages of the DAQ. The development of a framework for such real-time data processing for event selection is the second objective of this thesis. To achieve this objective we have to:

- Prove data can be processed in real-time using FPGA-based devices to extract features from FT relevant to the experiment.
- Prove it is possible to substantially reduce the volume of raw data using such a technique without sacrificing any crucial information from the data.

In order to fulfil the above goals the following tasks had to be completed:

- Develop an FPGA firmware that can reconstruct particle tracks for FT.
- Integrate the system with the FT read-out and test it under realistic beam conditions.

The study on the predetermined objectives is complete, and the findings are provided in the chapters, which are organized as follows.

Chapter 2 gives the physical motivation and research overview of the HADES and $\overline{\text{P}}$ANDA experiments. The chapter further describes the construction and the role of Forward Tracker in both experiments. The chapter ends with a brief introduction to the DAQ in HADES and $\overline{\text{P}}$ANDA.

Chapter 3 is dedicated to the read-out for FT. The chapter begins with the design goals for the FT read-out and describes the components responsible for signal

processing and digitisation. The tools and methods developed for the qualification of the read-out boards are discussed.

Chapter 4 describes the tests performed with the prototype FT detector system combined with the tests of the read-out under beam conditions. The track reconstruction tools, analysis methods and the obtained results are also discussed.

Chapter 5 is dedicated to the real-time data processing pipeline developed for the $\overline{\text{P}}$ANDA DAQ. The firmware framework and the components developed for processing FT data are described. The tests performed under beam conditions and the obtained results are presented in this chapter. Chapter 6 summarizes all the objectives attained in this study and talks about future ambitions.

Chapter 2

Forward Tracker in HADES and PANDA

2.1 Overview

2.2 FAIR facility

The Facility for Antiproton and Ion Research (FAIR) [5] is a new accelerator complex under construction alongside GSI Helmholtz-Centre in Darmstadt, Germany. It will be used for research with beams of heavy ions and antiprotons. The floor plan of the FAIR facility is shown in Figure 2.1. The primary machines at FAIR are the SIS-18 and SIS-100 synchrotrons with circumferences of 216 meters and 1100 meters, respectively. The SIS-18 allows accelerating ions up to the heaviest natural element, uranium, to energies of 1.5 GeV per nucleon. The positively charged ions produced in the Ion Sources at low kinetic energies are first accelerated by the UNIveral Linear ACcelerator (UNILAC) up to energies of 11.4 MeV per nucleon. To reach higher energies, the ions are accelerated further by the SIS-18. Afterwards, the ions can be used directly for experiments like HADES or produce a secondary beam of rare nuclei in the FRagment Separator (FRS). Furthermore, the setup involves the Experimental Storage Ring (ESR) storage ring that allows for the storage and cooling of accelerated ions. The SIS-100 will accelerate high-intensity proton and heavy ion beams with rigidity up to Z·30 GeV. The high-intensity heavy ion beam from the SIS-100 will also be used to produce secondary beams of radioactive nuclei, which will be collected, stored and cooled for further scattering experiments in a storage-cooler ring. The antiprotons will be produced in the facility by directing the 30 GeV/c proton beam from SIS-100 onto a copper production target. Antiprotons with momentum around 3.6 GeV/c will be collected in the Collector Ring (CR). Applying strong stochastic cooling to the beam reduces the momentum spread of the CRs antiprotons from $\Delta p/p \sim 3\%$ to $\sim 0.1\%$. Then, the beam will be transferred to the Recuperated Experimental Storage Ring (RESR). This will be repeated every 5 seconds until the 10^{10} - 10^{11} accumulated antiprotons will be injected into the High Energy Storage Ring (HESR).

The HESR is designed to accelerate/decelerate and store antiprotons in the momentum range from 1.5 to 15 GeV/c. Using stochastic and electron cooling systems, a high-quality antiproton beam will be produced by reducing the energy and emittance spread. HESR can work in two operation modes: a High Resolution (HR)

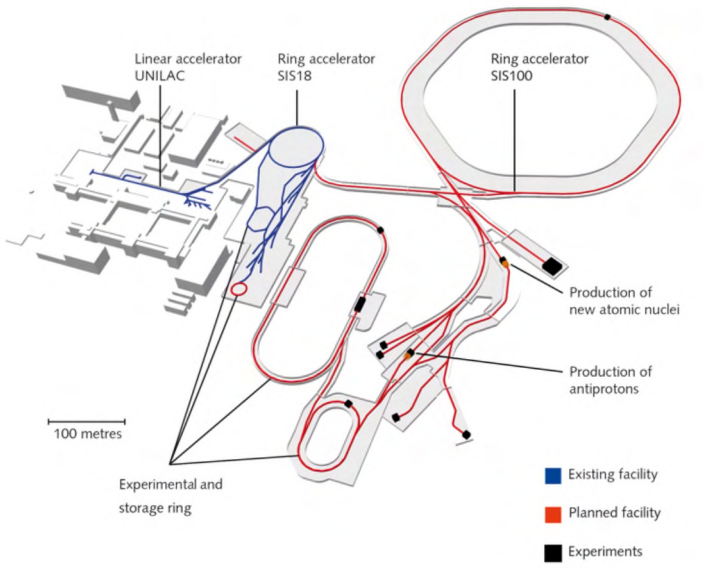


Figure 2.1: Future FAIR layout schematic showing existing GSI facilities on the left and additional installations, including the SIS 100 synchrotron, the storage and cooling ring complex with CR and HESR, and the Super FRS experiment, on the right [2].

mode with the beam momentum spread smaller than $\Delta p/p = 4 \cdot 10^{-5}$ (at luminosity $2 \times 10^{31} cm^{-2} s^{-1}$) for the 10^{10} stored antiprotons, and in a High Luminosity (HL) mode with a momentum spread of 10^{-4} (at luminosity $2 \times 10^{32} cm^{-2} s^{-1}$) but with 10^{11} antiprotons. The HR mode will be used to search for narrow states in formation reactions. The HL mode will be foreseen for production reactions with small cross-sections.

The FAIR facility allows several physics programs to be operated in parallel. These programs are divided into four major fields:

- $\overline{\text{P}}$ANDA - AntiProton ANnihilation at Darmstadt studies the field of physics with high-energy antiprotons.

- APPA - Atomic, Plasma Physics and Applications, which focus on investigations of properties of QED in the presence of strong electric and magnetic fields and matter under extreme conditions (i.e. high field, high pressure, high temperature). The atomic physics program will make use of atoms stored in ESR

- CBM - Compressed Baryonic Matter (CBM) to explore the QCD phase diagram in the region of high baryon densities. The research will be conducted by a new CBM detector and an already existing HADES spectrometer.

- NUSTAR - Nuclear Structure, Astrophysics and Reactions for investigating nuclear structure and dynamics. NUSTAR programme includes studies with radioactive beams produced by Fragment Separator (SFRS)

2.3 HADES and PANDA at FAIR

2.3.1 HADES

The High-Acceptance DiElectron Spectrometer (HADES) is a general-purpose, fixed target detector located at the SIS-18 accelerator at GSI. Its construction was completed in 2003 and is participating in the FAIR phase-0 program, continuing with its state-of-the-art physic program. After its completion, it will be moved to a new cave, where the CBM detector will be installed. The HADES physics program aims to explore the microscopic structure of dense baryonic matter. In particular, to understand the extent to which hadrons change their properties in QCD matter at high temperature and baryonic potential and when they ultimately lose their hadronic character. An essential part of this program is to carefully define the reference against the modifications of the measured hadrons. As primary probes, HADES uses virtual photons detected via dielectrons, which directly couple to the electromagnetic current of hadrons and the production of strange hadrons. The physics topics outlined for the FAIR Phase-0 physics program with HADES are listed below:

- Emissivity of baryonic matter via dilepton production.
- Search for in-medium modification of the light vector mesons by inspecting their line shape.
- Multi-strange baryon production.
- Electromagnetic structure of excited Baryons and Hyperons.
- Two-body particle correlations.

The HADES detector has a significant acceptance of 18°-80° in polar and almost full azimuthal angles for charged particles and is optimised to identify very rare electrons and positrons in a huge hadronic environment, which exceeds the electron signal by many orders of magnitude in multiplicity. The detector is built from different sub-detectors, focusing on particle identification and tracking, as shown in Figure 2.2.

The START is the first detector of the HADES experiment, exposed directly to the high-intensity beam, located in front of the first target segment. The time measured by the START detector is used as the time of the reaction after offset corrections. The VETO detector is located behind the target. It has an active area of 8 mm $\times$ 8 mm and is read out by eight pads. The VETO detector's primary purpose is to reject triggered events in which no nuclear reaction occurred in the target. The HADES Ring Imaging Cherenkov (RICH) detector is a hadron-blind Cherenkov detector whose primary duty is identifying electrons and positrons. RICH is equipped with a radiator (CF_4) which has a high threshold for the Cherenkov effect ($\gamma_{thr} = 11.2$) assuring that in the SIS18 energy range, only electrons produce light. The Mini Drift Chamber (MDC) provides tracking capabilities for the HADES experiment. It is built from 24 chambers in four layers and covers a polar angle of 18° to 85°. Each layer consists of six trapezoidal planar chambers placed inside six sectors of the superconducting magnet. The first two layers are in front of the magnet, whereas the last two are behind the magnet. MDC measures the bending

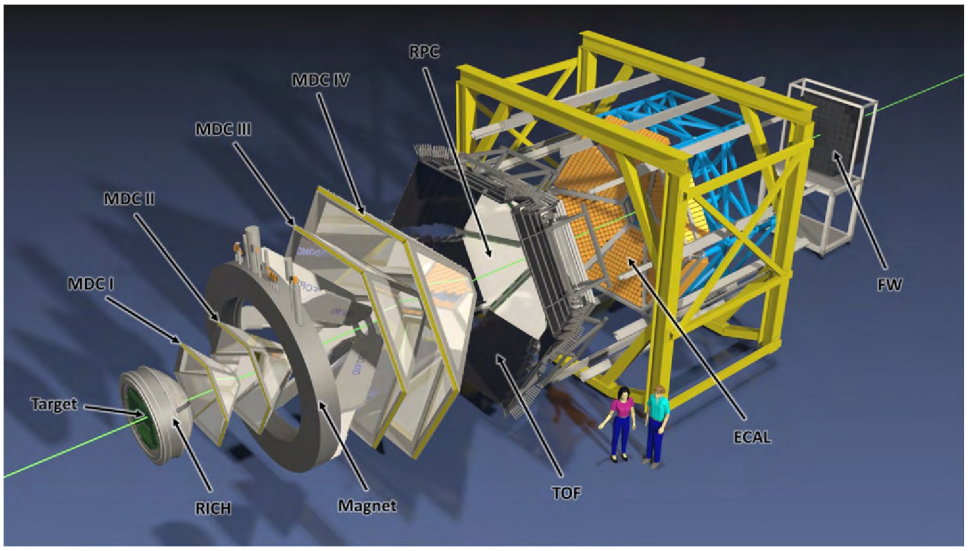


Figure 2.2: An exploded view of the HADES detector setup [6].

angle of a particle track that is related to particle momentum by means of a dedicated track reconstruction algorithm. The HADES detector uses two different detectors for the time of flight-based particle identification. The Time-Of-Flight (TOF) wall is one of those detectors based on scintillators, covering polar angles between 44° and 88°. The Resistive Plate Chamber (RPC) is the other TOF detector covering a polar angle of 18° to 45°. A lead glass Electromagnetic Calorimeter (ECAL), placed behind RPC, provides photon energy measurement and electron identification.

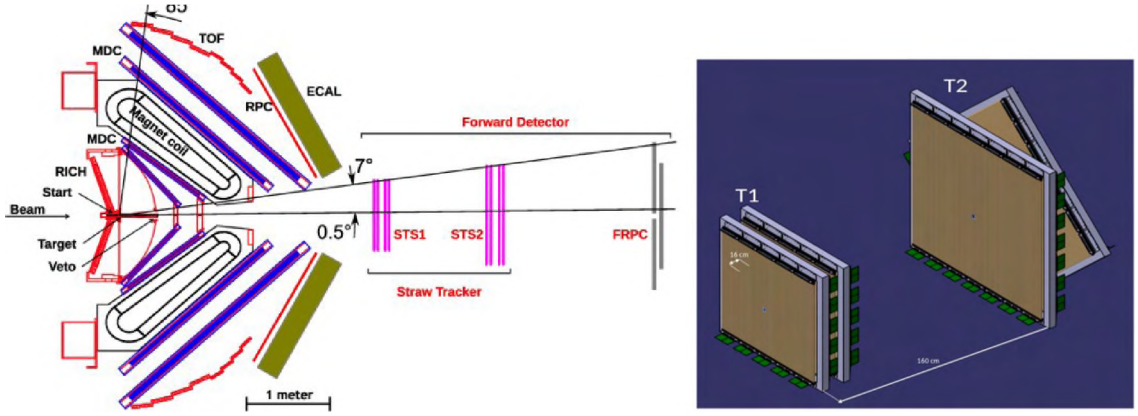


Figure 2.3: Left: Schematic side view of the HADES detector showing its compact design. The detectors are symmetrically arranged at the azimuthal angle around the beam axis [7]. Forward Detector system with the Forward Tracker and Forward RPC included. Right: Schematic representation of STS1 and STS2 station arrangement in HADES.

To extend the acceptance of the HADES Spectrometer towards lower polar angles, 0.5° - 6.5°, a dedicated Forward Detector (FD) has been constructed. This detection system consists of two tracking stations placed 3.1 and 4.6 m downstream of the target and is based on straw tubes, described in more detail below. It is followed by a high precision time-of-flight wall based on RPC technology or alternatively a high granularity scintillator-based hodoscope. This detector operates

in a field-free region, so no complete particle identification is possible. However, in the SIS18 energy domain, proton emission at forward angles is most probable. Hence, a proton particle hypothesis is assumed for the tracks reconstructed in FD. High-resolution time-of-flight measurement in RPCs allows for the calculation of the proton momentum.

Physics goals of the HADES FD

Two of the main physics goals of the HADES FD are to determine the total integrated luminosity of the experiment and to measure the electromagnetic decays of hyperon resonances in the region of a few GeV [8]. These goals are briefly discussed below.

The measured yields per second in an experiment depend on the accepted luminosity, the total cross-section of the studied process, and the angular distributions of the reaction products. The instantaneous accepted luminosity can be obtained using the equation described below:

$$\mathcal{L}^{acc}_{inst} = N_{beam} \times \frac{\rho}{A} \times N_A \times \varepsilon_e \tag{2.1}$$

Where N_{beam} is the number of particles in the beam (s^{-1}), ρ is the target density (gcm^{-1}), N_A is the Avogadro number (6.02×10^{23}), A is the atomic number of the target and ε_e is the total acceptance of data acquisition system (this is determined by many factors such as the fraction of time the beam is on target, the fraction of time triggers are taken, the dead time of the DAQ etc). Integrated accepted luminosity $\mathcal{L}^{acc}$ is the corresponding luminosity integrated over time of the experiment.

There is no detector in HADES to accurately determine the N_{beam} so it is not possible to calculate $\mathcal{L}^{acc}$ from eq.2.1. It can, however, be calculated by measuring the pp-elastic scattering yield of a well-known cross section using the equation below:

$$N^{pp} = \mathcal{L}^{acc} \times \sigma_R \times \varepsilon_{el} \tag{2.2}$$

Where $\mathcal{L}^{acc}$ is the accepted luminosity, N^{pp} is the total pp-elastic events in the polar angular range covered by HADES-FD ($0.5° - 7°$, σ_R is the corresponding elastic scattering cross-section ($4.44^{+0.8}_{-0.3} mb$), obtained from SAID database [9]) and ϵ_{el} is the total reconstruction efficiency of elastic scattering pairs in HADES-FD. The accepted luminosity can be thus calculated using the equation below:

$$\mathcal{L}^{acc} = \frac{N^{pp}}{\sigma_R \times \varepsilon_{el}} \tag{2.3}$$

As most of the protons from the pp-elastic scattering are emitted in the lower forward angles ($\theta < 7°$), FD is thus required for their identification and reconstruction of these pp-elastic events [7].

The FD also plays a big role in the physics programme of the HADES experiment related to measurements of higher mass hyperons production, i.e $\Lambda(1520)$, $\Lambda(1405)$, $\Sigma(1385)$, $\Xi(1321)$ and electromagnetic decays of $\Lambda(1520)$, $\Sigma(1385)$.

The hyperon production at a beam energy of 4.5 GeV is close to the production threshold. Consequently, hyperons are emitted at forward angles where HADES has no acceptance. Therefore, adding FD increase the acceptance of hyperon reconstruction. A dedicated simulation study of hyperon production and decays in $p+p$ collisions at 4.5 GeV [7], like, for example, $\Lambda \rightarrow p\pi^-$, $\Lambda^*(\Sigma^*) \rightarrow \Lambda e^+ e^-$ (hyperon

transition form-factors) and $\Xi^- \rightarrow \Lambda\, \pi^-$ demonstrate an increase of accepted decays by a factor of two (in the case of Ξ production, which is very close to the threshold, almost all accepted decays include proton in FD). The Forward Tracking Detectors included after the HADES upgrade can be seen in Figure 2.3.

HADES Forward Tracker

The HADES FT, a detector in the HADES FD, consists of two stations, STS1 and STS2, one behind the other, each composed of four double layers of self-supporting straw tubes of 10 mm diameter. STS1 has 704 straws, arranged in four double-layers with a tilt of 0°, 90°, 90°, 0°, respectively. It has a beam opening of 8×8 cm^2 and is placed 3.341 m from the target. STS1 has been built by Forschungszentrum Jülich. STS2 has 1024 arranged in 4 double-layers with a tilt of 0°, 90° 45°, -45° respectively, with an active region over 1 m^2. It has a beam opening of 16×16 cm^2 and is placed 4.910 m from the target. The STS2 has been built by the Jagiellonian University, Kraków. The best position resolution of the detector amounts to around 150 μm, which, for the given detector geometry, provides track reconstruction with an angular resolution of $\sigma_\theta = 0.5$ mrad for 2 GeV protons. The FT stations, STS1 and STS2 installed at HADES are shown in Figure 2.4. The STS1 - STS2 stations are prototypes of tracking stations of the PANDA Forward Spectrometer, described in more detail in the next section.

Figure 2.4: A photograph of STS1 (left) and STS2 (right) detector systems installed at HADES [7].

2.3.2 PANDA

The $\overline{\text{P}}$ANDA detector is an internal target experiment devoted to studies in the field of hadron physics by measuring reactions induced by scattering antiproton beams off a hydrogen target and off-nuclear targets [2]. The antiproton beam with momentum in the range of 1.5 GeV/c to 15 GeV/c will be provided by the HESR. The maximum momentum of the HESR antiproton beam corresponds to energy in

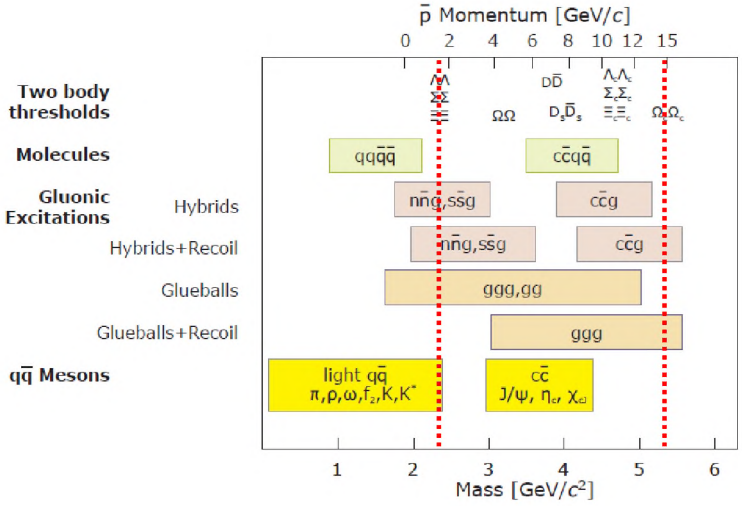


Figure 2.5: Overview of the accessible mass range (lower scale) for hadrons produced in $\bar{p}p$ collisions as a function of beam momentum (upper scale). The dashed red lines indicate the accessible momentum of antiproton beams at HESR and the corresponding mass range of the produced hadrons [10].

the centre of mass system of 5.5 GeV and is sufficient to produce pairs of charm quarks. Therefore, one of the primary research areas of $\overline{\text{P}}$ANDA is the spectroscopy of charmonium states and open charm mesons. Figure 2.5 shows the mass range of various states, which can be investigated at $\overline{\text{P}}$ANDA.

Besides studies of conventional mesons consisting of quark-antiquark ($q\bar{q}$)pairs, $\overline{\text{P}}$ANDA will also be used for a search for exotic mesons such as glue-balls (gg, ggg), hybrids ($q\bar{q}q$) and molecules or tetraquarks ($q\bar{q}q\bar{q}$). The $p\bar{p}$ annihilation is expected to be well suited for observing such exotic states due to the copious production of gluons. In experiments with hydrogen targets, the following primary research topics are foreseen:

- Spectroscopy of charmonium and open charm mesons.
- Search for gluonic excitations - hybrids and glueballs.
- Spectroscopy of charmed baryons.
- Spectroscopy of strange baryons (with double and triple strangeness)
- Study of nucleon structure by measurements of time-like form factors, Drell-Yan processes and generalised parton distributions.

In experiments with nuclear targets, PANDA plans to investigate [11]:

- Modification of properties of mesons embedded in the nuclear medium.
- Properties of single and double hypernuclei.

To pursue the planned physics program, the $\overline{\text{P}}$ANDA detector has to fulfil the following basic requirements:

- High rate capability necessary for measurements at the maximum interaction rate of the antiprotons with the target $\sim 2{\cdot}10^7$ per second.
- Close to 4π solid angle coverage, essential for Partial Wave Analysis.
- Identification of charged particles including pions, kaons and protons, electrons and muons with a wide momentum range.
- Good momentum resolution for charged particles of about 1.5% at 1 GeV/c.
- Detection of charmed meson vertices with a precision better than 100 μm.
- Electromagnetic calorimetry across a wide energy range.

PANDA is an asymmetric fixed target experiment with two components: the Target Spectrometer (TS) and the Forward Spectrometer (FS). The detector is shown in Figure 2.6.

Target Spectrometer

The TS, which is almost hermetically sealed to avoid solid angle gaps and which provides little spare space inside, consists of a solenoid magnet with a field of 2 T [12] and a set of detectors located inside a superconducting solenoid magnet that can measure the energy of neutral particles, the energy of charged particles, track charged particles, and provide PID information. The silicon Micro Vertex Detector (MVD) abuts the target area's beam pipe and provides secondary vertex sensitivity for particles with decay lengths of ≈ 100 μm. Surrounding the MVD in the central tracker is the Straw Tube Tracker (STT). In the forward direction, three tracking stations will be based on Gaseous Electron Multiplier foils (GEM) as the gas amplification stage. The tracking detectors like MVD and STT also provide information on the specific energy loss in their data stream. Two Detectors for Internally Reflected Cherenkov light (DIRC) are to be located within the TS. Compared to other types of Ring Imaging Cherenkov (RICH) counters, the possibility of using thin radiators and placing the read-out elements outside the acceptance favours the use of DIRC designs as Cherenkov imaging detectors for PID. The Barrel DIRC covers polar angles θ from 22° to 140° and is located inside the $\overline{\text{P}}$ANDA TS. It provides very good π-K separation up to 3.5 GeV/c (with at least 3 standard deviations). The End-cap Disc DIRC covers polar angles θ from 10° to 22° in the horizontal plane and 5° to 22° in the vertical plane. The tracking data is required to interpret the DIRC data because the Cherenkov angle is calculated between the direction of the Cherenkov photon and the momentum vector of the emitting particle. Small scintillator tiles measuring 3 cm make up the Scintillation Tile (SciTil) detector, which is mounted on a support frame outside the Barrel DIRC and will provide accurate relative timing and event start time. The EMC is subdivided into barrel detector, and backward and forward end-caps, all housed within the solenoid magnet return yoke. Besides detecting photons, the EMC [13] provides also electron identification. The $\overline{\text{P}}$ANDA TS's return yoke for the solenoid magnet is laminated to make room for multiple layers of muon detectors.

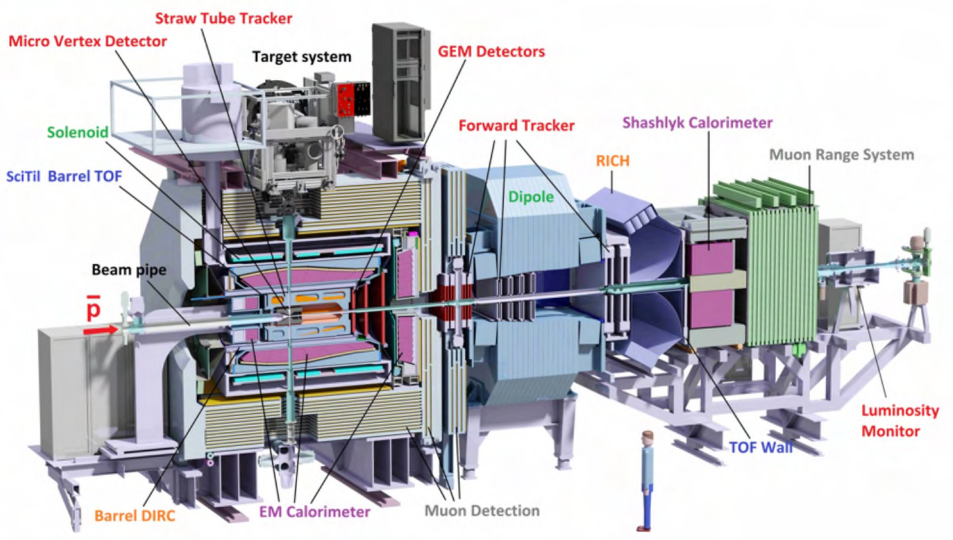


Figure 2.6: The Target Spectrometer (TS) is located on the left side of the $\overline{\text{P}}$ANDA setup's longitudinal section, and the Forward Spectrometer (FS), which begins with a dipole magnet on the right [2].

Forward Spectrometer

With a maximum value of ± 10 degrees horizontally and ± 5 degrees vertically relative to the direction of the beam, the FS angular acceptance has an ellipsoidal shape. The FS starts with a 2 Tm dipole magnet to provide bending power with a B-field perpendicular to the forward tracks. The magnet has a window frame with about a 1 m gap, a 3.1 m width and a 1.6 m length in the beam direction starting from 3.9 m downstream of the target. The dipole field will be ramped during acceleration in the HESR, and the final ramp maximum scales with the selected beam momentum. The magnetic field of the dipole magnet causes a deflection of the antiproton beam by an angle of 2.2°. The beam deflection will be compensated by two correcting dipole magnets, placed one upstream and the other downstream of the $\overline{\text{P}}$ANDA detection system.

Most of the detectors of the FS (except parts of the tracking detectors) are located downstream of the dipole magnet. FS consist of: a Forward Tracker with six straw tube stations, the Forward EMC of a Shashlyk-type and an aerogel RICH detector, located between the forward EMC and the dipole magnet. Furthermore, particle identification of slow particles, below the Cherenkov light threshold, is assured by a Time-of-Flight Wall. Near the beam pipe, a detector made of four layers of monolithic active pixel sensors picks up hits from the tracks of elastically scattered antiprotons to determine the luminosity.

$\overline{\text{P}}$ANDA Forward Tracker

The $\overline{\text{P}}$ANDA Forward Tracker (FT) is designed for the momentum measurement of charged particles deflected in the field of the dipole magnet of the $\overline{\text{P}}$ANDA Forward Spectrometer (FS) [10]. The $\overline{\text{P}}$ANDA FT consists of 12,224 straws arranged in three pairs of tracking stations: one pair (FT1, FT2) is placed before the dipole magnet, the second pair (FT3, FT4) inside the dipole magnet, and the third pair (FT5,

FT6) is placed after the magnet, as shown in Figure 2.7. Such placement allows precise parametrisation of the tracks of the particles bending inside the magnetic field. Each station will be made of four double layers of straw tubes. The first and the last layer are planned to be placed vertically, whereas the two middle ones will be skewed by ±5°. The straws included in the station will be grouped into modules. Each module will have 32 straw tubes equipped with individual power supply, gas distribution, high voltage and front-end electronics. The individual modules allow easy replacement of malfunctioning parts of the detector. The positions of the tracking stations along the beam line are indicated in the 3-D model presented in Figure 2.7.

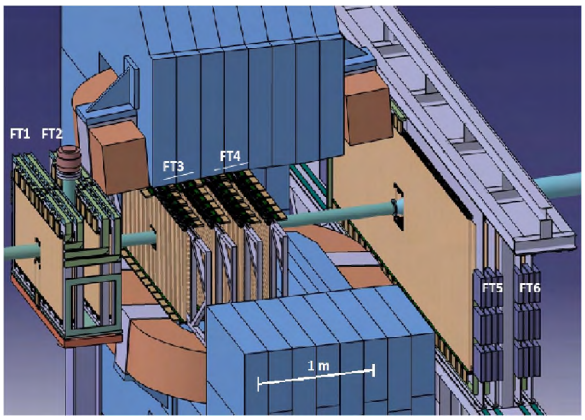


Figure 2.7: Forward Tracker stations (FT1-FT6) in the $\overline{\text{P}}$ANDA Forward Spectrometer with the dipole magnet [4].

2.4 Straw Tubes

The Forward Tracker (FT) is foreseen for tracking charged particles. The fundamental requirements for this tracker are based on simulations of selected benchmark channels and background reactions expected in $\bar{p}p$ and $\bar{p}A$ collisions. Some of the major requirements for FT straws are:

- The momentum acceptance of the tracker should extend up to 3% · p_{beam} where the lower limit is necessary for measurements of low momentum pions.
- good momentum resolution, comparable to or better than the one of the Target Spectrometer, which is about 1.5%.
- low material budget (< 5% X_0) to minimise the multiple scattering and the gamma conversions.
- high rate capability with particle fluxes up to $2 \cdot 10^7$/s at beam momentum of 15 GeV/c. The particle fluxes reach 25 kHz·cm $^{-2}$ in the vicinity of the beam-line.
- radiation hardness 0.1 - 1 C/cm per year.
- A high detection efficiency for a single particle hit ∼ 95%.

- fast front-end and digitising electronics capable of dealing with these high counting rates.

The straw tubes for the HADES and $\overline{\text{P}}$ANDA FT are designed after considering the above-mentioned requirements. These are self-supporting straw detectors, where the mechanical tension of the anode wire and the straw tubes is maintained by gas over-pressure and not by any external support frames. The straw tubes have a diameter of 10 mm and a total wall thickness of 27 μm. They consist of two 12 μm thick layers of aluminised Mylar film twisted around a rotating mandrel and glued together where they overlap. The tubes are aluminised at the inner and outer surface, which is used as the cathode. A gold-plated tungsten wire with a 20 μm diameter is used as the anode. End-plugs for these straws are designed for positioning and holding the anode wire. This has a cylindrical plastic bushing forming an essential mechanical element of the end plug, an aluminium ring for grounding the aluminised inner surface of the straw, a wire locator having a cylindrical shape with a V-groove for positioning the anode wire on the axis of the straw, a plastic plug fitting into the V-groove in the wire locator and a PCB for soldering the anode wire. A micro PVC tube is fed through a hole and glued into the end plugs to enable the gas to flow through the tube. The working gas mixture is of Ar + CO2 with a volume ratio (90: 10) [14]. The components of the straw and an assembled straw module are shown in Figure 2.8. Individual straw tubes are aligned with high precision also from the top by smaller reference plates, and then each tube is glued to the two adjacent ones at several defined points along its length. The second layer of straws is then carefully placed on top of the previous layer. A straw module consists of a planar double layer of 32 straw tube detectors supported by two end pieces. The straws are connected to the Front End Electronic Boards (FEB), and the high voltage (HV) supply is through one end-piece, whereas the gas mixture is supplied to the straws through the other in a daisy chain.

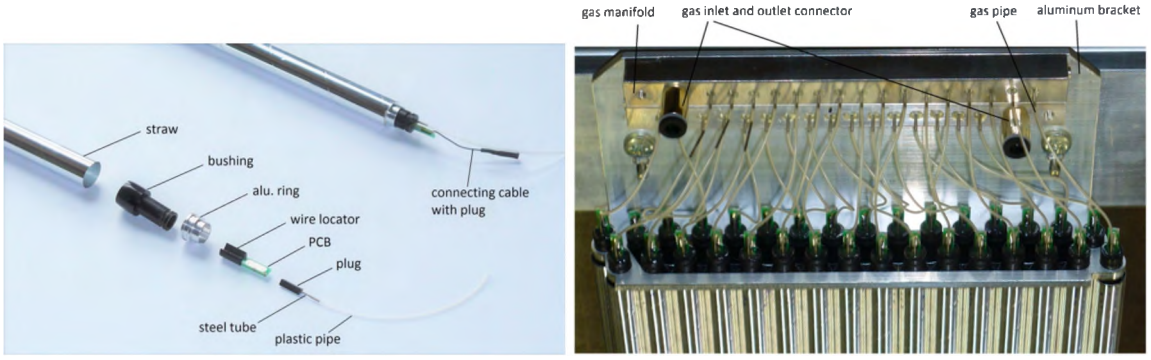


Figure 2.8: Left: Components of a straw tube (lower left) and assembled end-plug with attached connecting cable with plug (upper right). Right: A fully assembled straw module along with the attached end piece [14].

A particle passing through the straw tube ionises the gas molecules, producing electron-ion pairs. The high voltage applied between the cathode and anode causes the resulting ionisation electrons and positive ions to drift in the electric field to the anode and cathode, respectively. The longest drift-time (DT) corresponds to the maximum distance between the particle track and the anode wire (straw radius). The ionisation electrons reaching the anode wire are multiplied (by about 10^4) by

a strong electric field near the anode. During the ionisation, the number of created electron-ion pairs (primary ionisation) depends on the energy loss of the incident particle. The Bethe-Bloch formula shows that the minimum ionising particles (MIP) energy deposition in the Ar: CO2 (90:10) equals 2.5 KeV/cm at standard temperature and pressure. As straw tubes operate at 2 bars, the energy loss of incident particle equals 5 KeV/cm. This induces an electrical signal on the electrodes. These electric signals are later processed by dedicated FEBs.

2.5 Read-out and Data AcQuisition System

Read-out and DAQ are specialised engineering disciplines thriving mainly in the ecosystem of large science experiments. It mainly consists of electronics, computer science, networking and physics. It involves up-to-date technologies that deliver advanced detector sensors, signal processing chains (analogue and digital), data storage and some logic units that decide to store or discard any given data. Large-scale physics experiments use various detectors to gather the maximum amount of possible interesting information from a single physical event. Each type of detector represents a specific reaction to a given radiation type (e.g. charge particles, neutrals (photons, neutrons)) and its conversion into an output signal, generally an electrical impulse. Those responses depend on the type of detector and reactions; thus, each detector has to be equipped with a specifically designed read-out chain. All such subsystems have to be combined at some point into one unified system. The general building blocks of DAQ and its implementation in HADES and $\overline{\text{P}}$ANDA experiments are described in this section.

2.5.1 General structure

The exact form of read-out and DAQ depends on many aspects of the experiment (e.g. scale, physical phenomena to be investigated etc.). Although each experiment has different demands and approaches, the main structure of their construction is common. A dedicated detector system measures the reaction products, and the response of the detectors is then registered by specialised read-out electronics (Front-End Electronics) and transmitted to some storage devices for further analysis. These functional parts of the entire DAQ chain, from the detector itself to the final storage device, are shown in Figure 2.9. These parts are general enough to be applied to any system demanding processing data from some electronic sensors and are briefly discussed below.

- Detector: A sensor or a transducer that can convert the interaction of the detector material with a particle into some measurable electrical signals. A few main characteristics of a detector are sensitivity, response function, response time, energy-time resolution, dead-time and detection efficiency.
- Front-End Electronics (FEE): This is a general term used to describe a system that registers the electrical response of the detector and transmits it to the storage in an organised manner. The FEE can be split into two components:
  - Analog: The analogue FEE acts as an interface between the detector response signal and the digitiser. The nature of these detector electrical

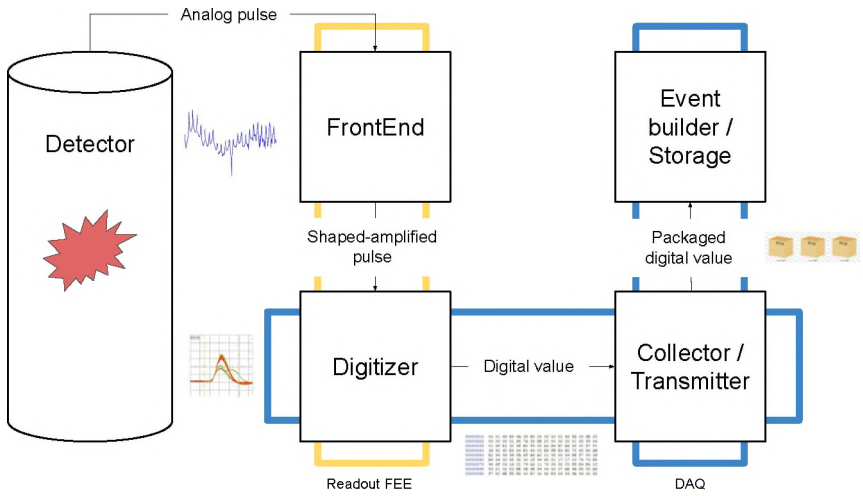


Figure 2.9: Building blocks of a single channel read-out chain. A physical event excites the detector to generate an analogue signal processing by shapers, digitisers, data collectors and transmitters. Event Builders save the output for offline analysis.

responses depends on the detector type and extends in time of duration from ns to micro-seconds and usually have small amplitudes (tens of mV). Fast shaping and amplification are required to measure these signals' time and amplitude (for charge measurement). For this reason, the analogue part of the FEE consists of signal amplifiers, shapers and in some cases, discriminators, followed by a digitisation unit. The analogue FEE is always placed close to the detector or directly attached to the detector to reduce signal losses and parasitic capacitance.

  - Digital: The digital FEE is responsible for translating the shaped signal from the analogue to the digital domain. Analog to Digital Converters (ADC) and Time to Digital Converters (TDC) are the most common forms.

- Data Concentrators (DC): The number of data sources (digital channels) in a large-scale physics experiment can be high (from a few thousand to millions). The data from the digital FEE has to exit the event-builders via a standardised network. Before entering the network, some hardware-based analysis is performed on the collected data. In the DC, the data exiting the digital electronics of the detectors are grouped, marked, packed and delivered to the component running analysis. DCs also gather data from trigger sources and slow control (see further).

- Network: Many subsystems in the experiment exchange data between modules and require a unified network infrastructure. For this reason, all the subsystems must be equipped with network gateways applying a chosen standard. Gigabit Ethernet [15] is one such popular example.

- Event Builders (EB): Event building is the task of reconstructing an entire event from all the small data coming from different sources (for example DC) in the whole system; it's the last step of concentration. Depending on the

system architecture and the online analysis algorithms, the reassembly can be realised either in the hardware or by the event-building computers.

- Trigger: The rate of physical events taking place in a detector system is often very high compared to the rate of events interesting for physicists. In that case, those events that are not interesting must be discarded. The mechanism of selecting events that are supposed to contain important information is called triggering. Trigger systems are hierarchical mechanisms that perform data filtering in several stages, passing only data to the next stage, proving positive for passing predefined tests. Each trigger stage introduces a more advanced method or algorithm to select only valuable events. A trigger well suited for the physics goal of the experiment is required for it to run efficiently.

- Slow-control: A mechanism that controls and monitors all the elements of the read-out and DAQ is called slow-control. It requires hardware facility, firmware and software to configure the parameters of the read-out process and monitor its behaviour. The hardware to be monitored or controlled should have a network interface. Using this, we can send and receive commands to a single or a group of selected elements of the DAQ using software on a PC.

A good read-out electronics and a data acquisition system is the key to efficient data collection. Designing such a DAQ system for any experiment should meet very high requirements.

2.5.2 FPGA in read-out and DAQ

As mentioned, detectors in high-energy particle physics experiments produce fast, tiny electrical signals that must be processed and recorded as data. It is the responsibility of the DAQ to interpret and reduce this data, which requires a lot of technological effort. The amount of work done in the hardware components of the read-out and DAQ has expanded mainly with the evolving semiconductor industry. Programmable Logic Devices (PLD) have been evolving to satisfy the increasing demands of the DAQ in high-energy physics experiments [16]. One of the most popular PLDs is the Field Programmable Gate Array (FPGA). The FPGAs offer the speed, density, computational power, flexibility and radiation tolerance required for these experiments. FPGAs have many advantages compared to other computing devices like CPUs and GPUs. Multi-core CPUs efficiently solve complex problems that can be divided into a few functional threads with mixed instruction sequences. The GPUs best calculate a very high number of the same operations with different data sets on each thread. The structure of FPGAs offers unique performance for real-time applications and online, parallel data processing with a limited arithmetic operation set.

The FPGAs are composed of three components. The Configurable Logic Blocks (CLB), programmable interconnects, and Input/Output (I/O) blocks. A CLB is made up of a Look-Up-Table (LUT), D-type Flip-Flop (FF) and a Multiplexer (MUX), as shown in Figure 2.10. A configurable Integrated Circuit (IC) can be designed by configuring the CLBs and their interconnections. Any logic gate operation can be achieved by setting up a truth table in the LUT. FPGAs have additional segments specialised for different tasks. For instance, Digital Signal Processing (DSP)

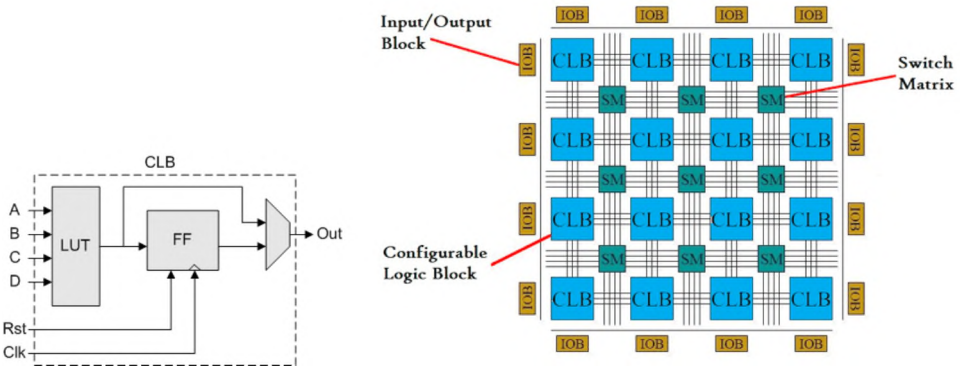


Figure 2.10: Left: An example schematic of a CLB. A truth table defines the output of the Look-Up-Table (LUT) and thus the output of the CLB. Right: Example schematic of an FPGA with its essential components. CLBs perform logic gate operations. To realise complex circuits, PSMs interconnect the CLBs. The I/O block routing (black outline) surrounds the array of the CLBs and connects the internal logic with the I/O pads.

slices use pre-implemented multipliers and accumulators to realise signal processing functions. The circuit design for the FPGAs is written in a hardware description language (HDL) like Verilog or VHDL. The next step generates a netlist describing the logic elements' physical distribution and the signals' routing. Later a configuration file called a bit file is created. The FPGA is configured with this file to perform the behaviour defined in the circuit design. Adaptability, parallelisation, communication and readily available IP cores make FPGAs a significant component of the read-out and DAQ. Using FPGAs, applications can be developed to run in real-time without interruptions. The only disadvantage is the complexity and the time required for each development cycle. In the HADES and $\overline{\text{P}}$ANDA experiments, FPGAs are used for FEE controls, monitoring, signal processing, data compression, high-speed data links, and online reconstruction and selection of the collision events. In the context of this thesis, FPGAs are used extensively in developing the read-out and DAQ of the FT described in Chapter 4 as well as in the development of the data processing pipeline described in Chapter 5.

2.5.3 Trigger Readout Board (TRB)

Trigger Readout Board (TRB) [17, 18, 19] is an FPGA-based multi-purpose detector read-out platform designed by the GSI Helmholtzzentrum für Schwerionenforschung, University of Frankfurt and the Jagiellonian University Kraków, for a wide range of digital applications. An FPGA-centric hardware architecture, well-defined network protocols, firmware modules for intra and extra-FPGA communication, and software tools to interface the system functionalities make the TRB a complete system for DAQ applications. The most popular configuration of TRBs performs precise time digitisation in multichannel TDC, that is implemented in FPGA and serves for timing applications. However, due to the flexible and re-configurable capabilities of FPGA and the flexibility of add-on extension cards, it can perform also other tasks like for example amplitude measurements. Thanks to these features, TRB has become a general-purpose device that can be used as a stand-alone board or as a part of a complex read-out system. The TRBs' hardware, firmware, and software

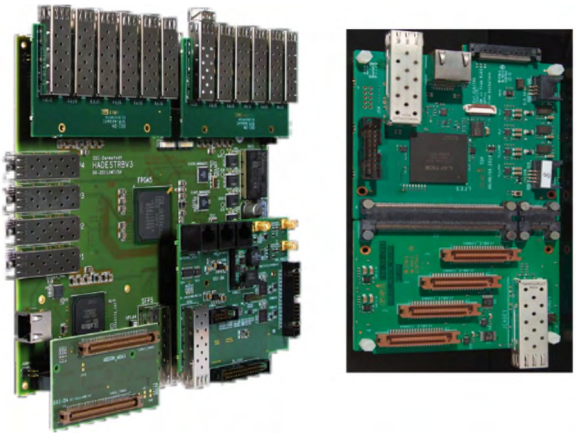


Figure 2.11: Left: TRB3 equipped with different extension modules [19]. On top are two SFP mezzanine add-ons plugged; down left is an Analogue Digital Analogue (ADA) mezzanine add-on, and on the downright Multi-test mezzanine add-on. Right: TRB5sc equipped with a 4-connector 16 LVDS channel pair add-on.

aspects are further discussed.

Hardware

The TRB hardware comprises two main elements: carrier boards and extension cards. The carrier board provides basic functionality like data collection and slow-control and can be interconnected to build larger systems. Extension cards (add-on cards) [19] are modules developed for dedicated applications, including a common connector and interface to the carrier board. They are the interface to detector FEB or directly to detector channels. The most popular carrier boards are the TRBv3 and the TRB5sc shown in Figure 2.11. TRBv3 has five Lattice ECP3-150EA FPGAs arranged in a star-like architecture where the central FPGA is used as the common control unit for the rest of the system, while the recent TRB5sc uses only one advanced Lattice ECP5 FPGA in a smaller form factor.

The logic architecture of the TRB system is composed of hubs and endpoints. The hubs implement communication features to distribute triggers, slow control commands and gather read-out data. The endpoints interface with the hubs and send data upon reception of a trigger. The system is arranged in a hierarchical tree structure with one master hub as a root to which additional hubs or endpoints can be connected. Multiple FPGAs on a single board fulfil such architecture, with one central FPGA being a hub and peripheral FPGAs acting as endpoints, all connected in a star-like topology. Multiple boards can be interconnected with optical fibres through 2 Gbps SFP to construct systems of a larger scale. Utilising these aspects, a TRB can be configured for a particular application and be used at various stages of the read-out system.

Firmware

The functionality of a TRB is defined by the firmware of the FPGA. It consists of modules for inter-FPGA communication, network protocols, and data concentration (DC) that are common for all applications [18] and custom modules for user-specific

functions like a TDC, ADC, read-out request distribution, etc. TrbNet [20] is a network protocol in the TRB framework developed for the internal communications of the TRB system components. It is also responsible for the distribution of read-out requests, read-out data transport, and exchange of control and monitoring messages. As each process has a dedicated priority and bandwidth requirement, TrbNet recognises the data type and manages the operations. The protocol runs on bi-directional lines between Printed Circuit boards (PCB), optical fibres, or copper cables. The FPGA configuration on the TRB can be dynamically re-programmed via TrbNet by transferring a bit-file (design configuration for the FPGA) to the attached Flash memory and initiating FPGA reload command.

Software

The TRB framework is completed with software packages developed for the interactions between the user and the components of the TRB system. TrbNet functionalities are controlled using the register read-write operations that are interfaced with software packages based on C and Perl. The TrbNet binding is used for the software to communicate with any endpoint or hub in the network for operations like slow control, flash programming the FPGA, read-out requests, reset of the system, etc. A JavaScript-based web GUI has also been developed to monitor the hardware, and read-out procedure [18]. These tools provide valuable information about the status of the setup, data rates, and hit rates in the detector that is auto-updated in configurable intervals. The framework's hardware, firmware, and software components are combined and built into a unified read-out architecture suitable for large-scale detector read-out applications.

2.5.4 HADES DAQ

The HADES DAQ is designed to handle data rates up to 300 kHz and a total data rate of up to ≈700 MBytes/s. Three main components of HADES DAQ are the FEEs that digitise the detector signals, the Central Trigger System (CTS) and the Event Builders (EBs) [20]. HADES DAQ uses TRB extensively, mainly in digitising units, network hubs and trigger distribution. The complete DAQ network setup consisting of the components is shown in Figure 2.12. The trigger and read-out process for the full system is controlled by the CTS. In parallel to the data network, a set of signals retrieved from the FEE of detectors are being transported to the units analysing the physical relevance of the FEE signals. The Baseline Recovery unit (BLRSum), secondary trigger-box and primary trigger-box are three such units. The BLRSum performs a sum of analogue signals from RPC and TOF detectors and provides a discriminated logical output. The secondary trigger-box performs coincidence checks on signals from ECAL, STS, fRPC and the Veto detector. The outputs from the detector FEE, BLRsum unit and the secondary trigger-box all arrive at the primary trigger-box. Here, a special trigger logic or combinations of trigger logic relevant to the physics study case can be configured—for example, the presence of a certain number of hits in different detector regions. The CTS receives a positive trigger decision from the primary trigger box and distributes it to the detector FEE. It sends also a global reference time signal to assure synchronisation of FEE (for example time measured in TDCs can be calculated w.r.t this reference time). This starts the read-out of the data from the respective detectors and sends them to the

EBs via a global gigabit switch. When the FEEs have finished the read-out and transmitted the data, they notify the CTS system. Only after all FEEs finished the read-out and notified the CTS can the next trigger decision be taken.

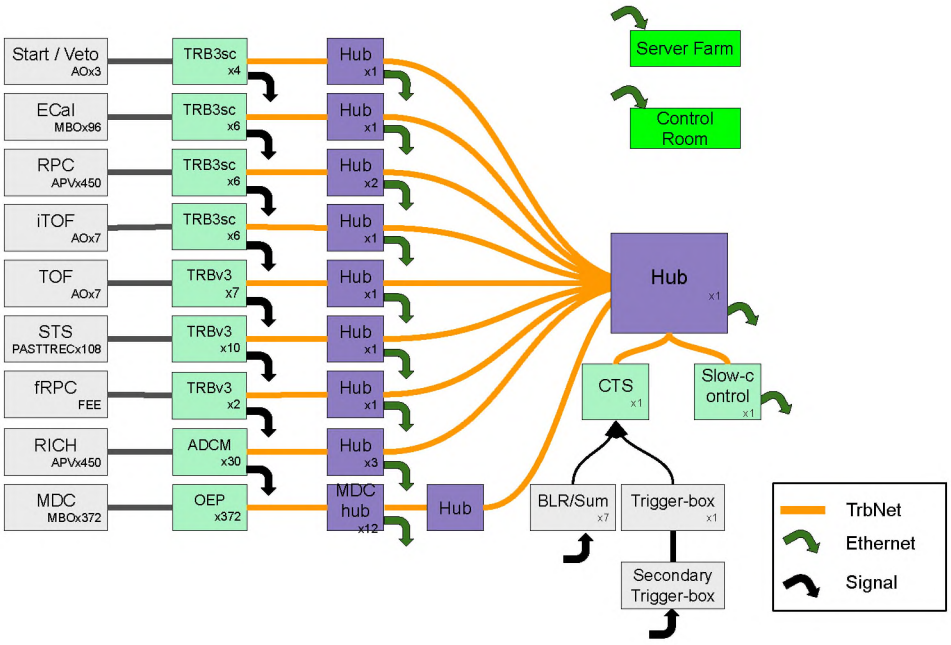


Figure 2.12: A schematic view of the HADES DAQ network setup. Network hubs are shown in purple, and all read-out boards are green. Additional front-end electronics are shown in grey. The small numbers indicate the number of boards of each type in the DAQ system.

All the FEEs in the detector system are connected using a dedicated network. The network is organised in a tree-like structure, with one central hub connecting the CTS and the slow control interface to other systems. From the central hub, the network is separated into subsystems, which are again connected using additional hubs. This separation gives the possibility to run each subsystem individually during test periods. The backbone of the DAQ system is formed by a set of servers ("Event Builders") which collect data from all subsystems, combine it into one data block and write it to the data storage. First, data is stored on local hard drives and transported to tape or disk storage in the GSI computing centre. A central 10-GbE network switch connects all systems to the server farm and the computing centre. The EBs collect all data and write them to disk in the HADES List mode Data (HLD) file format. The HLD data format is further described in Section 4.3.2.

DAQ for HADES FT

The electric signals of HADES FT are processed by dedicated FEBs connected directly to the detector. The FEBs are equipped with two 8-channel charge-sensitive ASICs called PASTTREC ($\overline{\text{P}}$ANDA Straw Tube Tracker Readout Chip) [21]. Here the signals are shaped, amplified, and discriminated with a common threshold set by an integrated Digital to Analog Converter (DAC). Characteristics of PASTTREC are described in detail in Section 3.2. The HADES FT is a two-station setup with STS1 that has 704 channels and STS2 has 1024 channels to be read out. STS1 is equipped

with 44 (88 PASTTRECs), and STS2 is equipped with 64 FEBs (128 PASTTRECs). TRBv3 is used as the digitising platform for the FT PASTTRECs. The rising and falling edges of the fast LVDS signals from PASTTREC discriminator outputs are measured using TDCs implemented in the TRBv3. The peripheral FPGAs (four) in the TRBv3 is configured with 48 channel TDCs (20 ps RMS time resolution) each. There are four TRBv3 for the read-out of STS1 and six for STS2. The data collected in the TRBv3 is sent to the central hub over the TrbNet and further to the EBs over the Gigabit Ethernet. The components of HADES FT DAQ are shown in Figure 2.13. Alongside the digitised data, TRBv3 in the FT read-out provides also logical signals required for the trigger generation. These signals are sent to the secondary trigger-box for coincidence and multiplicity checks. The resulting outputs are sent to the CTS. A software package has been developed for controlling and monitoring the FEBs in the FT, further described in Section 3.4.2. All the FEBs in the FT read-out are configured/controlled using the slow-control module in the TRBv3, and this software is installed on the computers at the HADES DAQ control room.

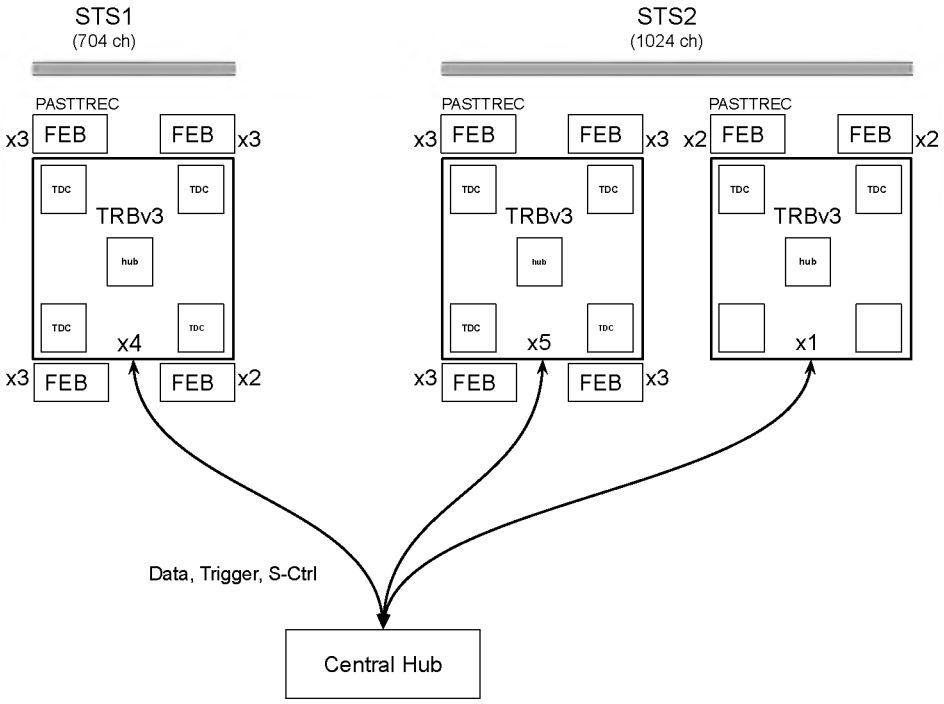


Figure 2.13: Schematic view of the DAQ system for the HADES Forward Tracker read-out. 16 channel FEBs (2 PASTTRECs) are connected to a TRBv3 with a $\approx$ 10-meter long 40-pin ribbon cable. The TRBv3 is connected to the network hub using full-duplex optical fibre to move data, trigger and slow-control commands.

2.5.5 PANDA DAQ

The $\overline{\text{P}}$ANDA experiment will operate at high beam-target almost continuous (see below) interaction rates reaching 20 MHz [2]. DAQ system with a continuous detector read-out is assumed. The data stream of about 200 GB/s [10] will be inspected online to search for various pre-defined event topologies corresponding to physics

channels of interest. The continuous read-out allows for such flexible measurements. However, the large amount of raw data has to be significantly reduced already in the initial stages of the $\overline{\text{P}}$ANDA DAQ. With this in mind, the DAQ for $\overline{\text{P}}$ANDA is designed with three major components: detector read-out Front End Electronics (FEE), Data Concentrators (DC), network infrastructure and Online Processing Nodes (OPN) for synchronous event processing, as shown in Figure 2.14.

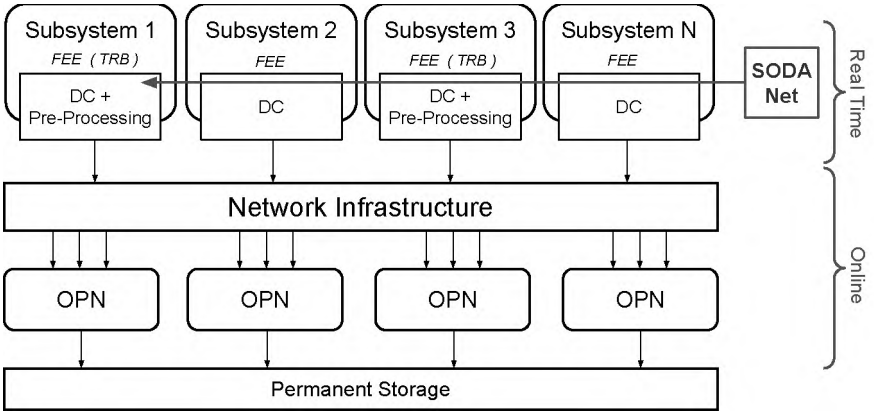


Figure 2.14: The overview of the $\overline{\text{P}}$ANDA read-out system along with the pre-processing pipeline in the Data concentrators (DC) for TRB-based detector systems and Online Processing Nodes (OPN) for synchronous event processing.

The FEE detects particle hits, prepares raw analogue signals, and performs digitisation in dedicated units. The TRB introduced in Section 2.5.3 is an example of one commonly used digitisation component in $\overline{\text{P}}$ANDA FEE.

The Straw Tube Tracker (STT), Forward Tracker (FT) and Barrel Detection of Internally Reflected Cherenkov light detector (DIRC) are some of the detector subsystems in $\overline{\text{P}}$ANDA that will use the TRB for time measurement. The digitised data from the TRB are sent to the DC. The DC is designed to collect the digitised data from all the FEEs belonging to a subsystem and distribute detector synchronisation signals. Both data collection and synchronisation signal distribution are done using a protocol called Synchronisation Of Data Acquisition Network (SODANet) [10, 3] by providing a common clock signal and time-stamps for all $\overline{\text{P}}$ANDA subsystems. To reconstruct a complete event from many data fragments, each fragment must be marked with an exact time stamp. This is a two-step process. First, the packets containing time-stamp information are sent to each Data Concentrator (DC). Secondly, the clock signal from the transmission is recovered and is used for DC logic synchronisation. This approach assures that the DCs and FEE are synchronised to the same clock for all $\overline{\text{P}}$ANDA units.

This section of the DAQ uses custom hardware common to all $\overline{\text{P}}$ANDA subsystems and should operate in a real-time regime. The network infrastructure transmits digitised data from all the $\overline{\text{P}}$ANDA subsystems. The data packets belonging to the same time frame are sent to a single OPN for further online analysis. The OPN will perform processing of complete time frames from all the subsystems using various algorithms implemented in CPU and GPUs. In the experiment, the interaction of the antiproton beam with the internal proton target will last for 2 μs. An interval of 400 ns will follow it. This interval is used to gain time for the data processing. Such a 2.4 μs cycle is called a burst, and 16 such bursts make up one' super burst.

Detector data are read out from the DC on each super-burst update i.e at ∼26 kHz (SODANet frequency) [10, 3].

A solution for real-time data processing in FT for TRB-based DAQ systems has been developed by the author of this thesis and its architecture is presented in more detail below.

DAQ for $\overline{\text{P}}$ANDA FT

The expected hit rates per channel in the $\overline{\text{P}}$ANDA FT can reach 350 kHits/s. The read-out described in Section 2.5.4 for HADES FT is incapable of coping with such data volumes; therefore, a new hardware platform is required. For this purpose, the latest hardware in the TRB family called TRB5G is used. It is equipped with a more advanced FPGA in a smaller form factor (ECP5UM) which is an evolution of the existing ECP3 FPGA on the TRBv3 platform. The TRB5G hardware is also around four times smaller compared to TRBv3. TRB5G is mountable on a crate system that includes a back-plane for communication and power supply. Resources available in the ECP5G FPGA devices allow for implementing up to 64 low-resolution (below 0.5 ns) TDC channels sufficient for the read-out of 4 PASTTREC FEBs. The data format of the TDC comprises one 32-bit word containing: the channel number, leading-time (relative to the burst up-date signal from SODANet) and its width for the TOT measurement. It is a significant (more than factor 2) data volume reduction compared to the TDC used in the DAQ for HADES FT (TRBv3).

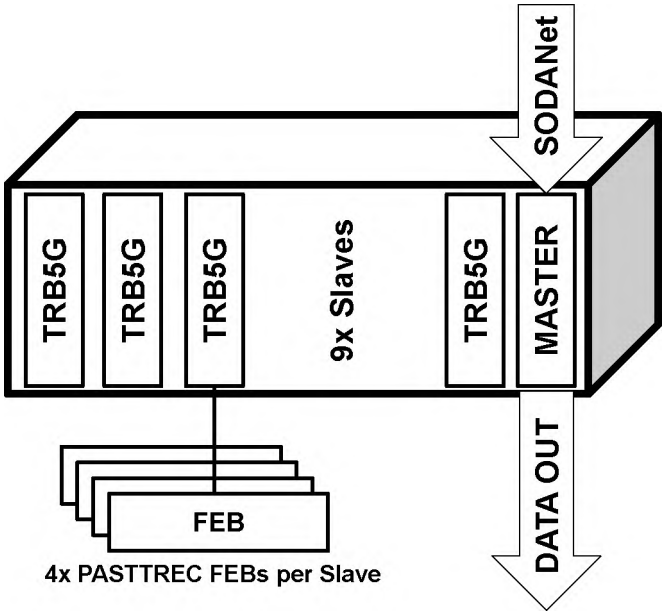


Figure 2.15: TRB5 G-based read-out architecture for $\overline{\text{P}}$ANDA FT.

Each TRB5sc will be mounted on a custom crate as shown in Figure 2.15. Each crate will house a master board which acts as an interface between the slave TRBs in the crate and the DC. The DC will function as a bridge between the output of the master board and the network infrastructure. The data in the DC are stamped with time information, synchronised and read out to the network infrastructure at a rate defined by the SODANet. The proposed intermediate pre-processing pipeline

in the DC has to unify the data streams from master boards arriving at the DC and filter the data before they are sent over the network.

	FT 1,2	FT 3,4	FT 5,6
No. of channels	2304	3328	6592
Average hit rate per straw	35 kHits/s	31 kHits/s	9 kHits/s
TRB5sc's	36	52	103
Master boards	4	6	12
Total bandwidth	324 MB/s	410 MB/s	237 MB/s

Table 2.1: $\overline{\text{P}}$ANDA-FT read-out requirements.

The number of TRB5sc, master boards and expected data rates for each $\overline{\text{P}}$ANDA FT station pair are presented in Table 2.1. The components of the FT read-out are further discussed in detail in the upcoming chapters.

Chapter 3

Read-out system for Forward Tracker

The Front End Electronics Board (FEB) is a general term for a collection of electronics that converts the signal directly from the detector into a digital form that can be stored on an archiving device for further analysis. The FEB for particle detectors generally consists of a signal amplifier, shaper and for time measurements discriminator, followed by a digitisation unit. The latter is either ADC (Analogue to Digit Converter) or TDC (time to digit conversion). The FT in $\overline{\text{P}}$ANDA is a tracking detector, and the FEB is required to provide the drift-time and the ionisation charge of a particle passing through the detector. The $\overline{\text{P}}$ANDA Straw Tube Tracker Readout Electronic Chip (PASTTREC ASIC) is an 8-channel ASIC developed by AGH-JU [21], especially for the straw tube detectors. Two ASICs are located on FEB and connected directly to a straw tube module. The design goals for the FT read-out, characteristics, methods used for the quality control and the recent optimisations are described in this chapter, along with the results from the in-beam tests.

3.1 FEB Design goals

3.1.1 Electrical properties of Straw Tubes

The most important parameters for the PASTTREC are the sensor capacitance, signal amplitude, shape and length, and electronic noise. The ASIC has to be designed so that its input characteristics match the electrical properties of the detector, operating conditions and expect count rates. These electrical properties of the straw tubes are listed in Table 3.1.

The straw length can vary between 40 cm to 150 cm, with a maximum capacitance of ≈14 pF. The straw tube acts as a coaxial transmission line from the pulse propagation point of view, with the impedance given by:

$$Z = \sqrt{\frac{R + i\omega L}{i\omega C}} \tag{3.1}$$

For high frequencies (>100 MHz), the impedance of the straw tubes tends to the limit at:

$$Z \to \sqrt{\frac{L}{C}} = 373\Omega \tag{3.2}$$

Table 3.1: Electrical properties of straws in FT

Capacitance	8.9 pF/m
Sense wire Resistance	258 Ω
Inductance	1.24 μH/m
Impedance	373 Ω
Analogue cross-talk	$\leq$ 1 %

The straw tubes in the FT can be compared to a capacitor holding charge Q_{det} = C_{det} * U_{HV}, where U_{HV} is the high-voltage applied to the anode of straw and C_{det} is the internal capacity of the detector. A high voltage is applied between the cathode and the anode in the straws. The electrons and positive ions separated by the particle passing through the detector drift in the electric field towards the anode and cathode, respectively. In the vicinity of the anode wire, the field strength becomes large enough to produce an avalanche, further multiplying the separation of electrons and positive ions. After the electrons are collected at the anode and the ions are neutralised at the cathode, the capacitor's charge (C_{det}) is diminished by the exact same amount of charge that was separated in the avalanche. Since the detector capacitor is connected to an external voltage source (via the FEB), it is recharged to its original charge state. This recharging current is registered by the feedback capacitor of the operational amplifier as the detector signal. Therefore, the voltage observed in the output of the FEB depends on the internal capacity of the detector C_{det}. It induces the need for capacity compensation as it can change with the detector dimensions, temperature or the age of the detector. Such compensations are not trivial and are a severe drawback. The idea is to use a charge-sensitive amplifier and later integrate the charge on the feedback capacitor of this operational amplifier.

3.1.2 Requirements for the FT analog FEB

Hit rates

The FT at $\overline{\text{P}}$ANDA is expected to experience a maximum counting rate of 1400 kHz for the straws located close to the beam-line in the first tracking station (FT1) at the highest beam momentum of 15 GeV/c and at $\overline{p}$p interaction rate of 2×10^7/s. The counting rate decreases from the maximum with increasing distance from the beam axis. PASTTREC must be able to process the signals generated at these hit rates and avoid the pile-up effects. The maximum drift-time for electrons in the tracking stations FT1, FT2, FT5, and FT6 (straw tubes situated outside the magnetic field region) is 130 ns. In the straw tubes working in the magnetic field of the dipole magnet, reaching up to 0.9 T (tracking stations FT3 and FT4), it extends to about 180 ns. The maximum duration of the analogue pulse should be comparable to the maximum drift-time and signals should be well separated even at hit rates of 1400 kHz. PASTTREC should withstand a maximum radiation dose of 5 krad, which will be accumulated during the lifetime of the $\overline{\text{P}}$ANDA experiment of 10 years [2].

Dynamic range

The PASTTREC uses a charge-sensitive amplifier with a feed-back loop integrating the charge on a capacitor as described in Section 3.1.1. This means that the charge ionised by the particle passing the detector corresponds to the amplitude of the signal. Around 200 electron-ion pairs are produced by a Minimum-Ionising Particle (MIP) in the straw tubes. The detector's high-voltage of 1800 V generates a gas gain of 5×10^4 resulting in 10^7 electrons. Hence, the total charge of 1600 fC can be calculated from the equation :

$$Q = 200_{primaryelectrons} \times G \times 1.6 \times 10^{-19} \tag{3.3}$$

where

$$G = e^{0.009U - 5.3525} \tag{3.4}$$

The PASTTREC is expected to have a large dynamic range, capable of measuring the charge deposited by the MIPs and slow protons and kaons with a factor of 4 to 5 larger energy deposition. Moreover, a good position resolution requires the detection of a single ionisation cluster which consists of 1 to 2 electrons corresponding to a charge deposition up to 5 fC. This way, the intrinsic noise level should also be below 1 fC, and the discriminator threshold has to be as low as possible.

Time-Over-Threshold approach: baseline, peaking-time and gain

As mentioned earlier, the FT in $\overline{\text{P}}$ANDA is a tracking detector, and PASSTREC is required to provide the time and charge information of a particle passing through the detector. TOT is defined as the time difference between the signal's leading and trailing-edge at the applied discriminator threshold.

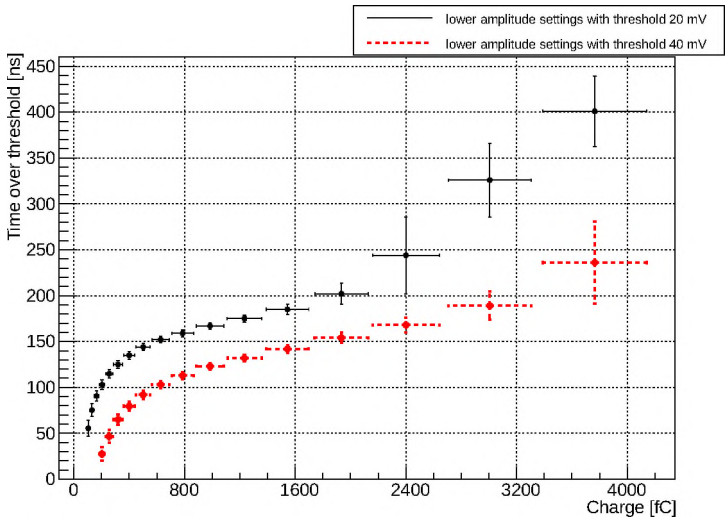


Figure 3.1: TOT and charge correlation obtained by taking into account the number of primary electron production amplified in the straws. The TOT values come from Gaussian distribution fitted to the TOT spectrum which was collected with a ^{55}Fe source [3].

It bases on the fact that the amplitude of the signal from the straw tube detector is correlated to the width of the signal above some voltage level called the

discriminator threshold. This approach is mainly cost-resource practical and simpler than signal integration methods used in QDCs or high-speed sampling used in ADCs. It has earlier been proven successful by the straw tube detectors in the ATLAS experiment [22]. The shape and position of a signal are very important as they directly translate to the time and energy of the charge induced in the straws. The HADES-$\overline{\text{P}}$ANDA straw tubes have a drift radius of 0.505 cm and a drift-time resolution of 1 ns. Therefore, every ns difference in the lead-time can cause roughly a difference of $\approx 30\mu$m in the reconstructed position of the particle track. Time Over Threshold (TOT) is a technique that can be used to get both the time and the charge information from the signal generated in the straws. The correlation between the charge induced in the straws and the TOT is shown in Figure 3.1.

Table 3.2: Requirements for the FEBs used in $\overline{\text{P}}$ANDA FT [14]

peaking-time	$\leq$ 40 ns
Double pulse resolution	$\sim$ 100 ns
Intrinsic electronic noise	$<$1 fC
Discrimination threshold	$\approx$5 fC
Max. counting rate	1400 kHz
Radiation dose (10 years)	5 krad

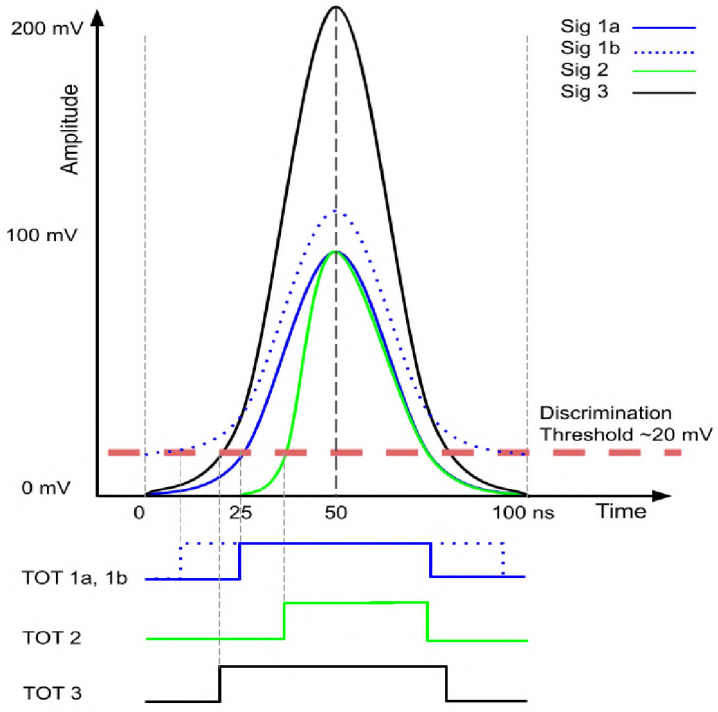


Figure 3.2: Schematic representation of various FEB signals discriminated at 20mV. The difference in lead-time and TOT caused the due change in baseline position (sig 1a, 1b), peaking-time (sig 2) and gain (sig 3) is presented.

The baseline of a signal can be defined as a point from where the signal begins and ends. When a common discrimination threshold is applied across all the channels in the detector, the nature of TOT can differ a lot if the baselines of the FEB channels are not uniform, as shown in Figure 3.2. For instance, signals 1a and 1b

in the figure are the same, except the baseline is shifted by a few mV leading to a significant difference in the TOT. For this reason, the channels must have a uniform baseline level and stability, particularly at high rates.

Peaking-time is defined as the time required by the shaped pulse to go from the baseline to the peak. The 'lead-time' of a signal determines the position of the particle passing through the straw. Signal 2 in the figure compared with signal 1 shows the difference in the lead-time and consequently the TOT due to the change in the peaking-time. With the increase of the peaking-time, the time precision of the measured signal decreases. However, the signal-to-noise ratio improves, thus making it very important to have the signal with an appropriate peaking-time. For this reason, the PASTTREC must have a configurable peaking-time which has to be optimized in the given experimental conditions. From the previous tests conducted with straws connected to fast sampling ADCs, it was concluded that peaking-time should be below 40 ns [23].

The lead-time and the TOT of the detector signal can vary due to different ionisation in the straw induced by passing particles. The difference in the measured lead-time emerging from the difference in the signal amplitudes is called "time-walk" and cannot be avoided (it can be in principle corrected for in off-line analysis knowing particle velocity and track length). However, the "walk" effect can also be induced by variation of the gain in the charge-sensitive pre-amplifier of PASTTREC. This is visualized in Figure 3.2 where signal 3 is compared to Signal 1a. For this reason, it is essential that all PASTTREC channels have uniform gain characteristics leading to good time-precision and signal-noise ratio.

The basic requirements of PASTTREC for the FT straw tubes are listed in Table 3.2. The signal processing requirements of the FEB are further described.

Signal shaping

The electrons separated in the avalanche accelerate more rapidly in the electric field than the positive ions due to the difference in their mass and mobility. The current signal generated in the straw detector has a fast (ns range) electron component and a slow (μs range) ion movement component. The total induced charge Q^{ind} at a time 't', by the movement of the N_{tot} is of charge $+e_0$ in a straw tube with radius 'b' and anode wire radius 'a' is given by:

$$I_1^{ind}(t) = -\frac{N_{tot}e_0}{2\ln(\frac{b}{a})}\frac{1}{t+t_0} \tag{3.5}$$

$$Q_1^{ind}(t) = \int_0^t I_1^{ind}(t')dt' = -\frac{N_{tot}e_0}{2ln(\frac{b}{a})}\ln\left(1+\frac{t}{t_0}\right) \tag{3.6}$$

Where 't_0' is the characteristic time constant, which will be a few nanoseconds in practical cases.

The slow signal from the positive ions leaves a long amplitude tail up to several microseconds making the integration of the total charge not feasible, as shown in Figure 3.3. It would significantly increase the detector's dead time and reduce high-rate capability. Therefore, the read-out has to compensate for the conditions where signal amplitude is measured at high event rates; otherwise, if two signals arrive close in time, then the second signal may start on the tail of the previous one causing a pile-up. This pile-up contradicts the PASTTREC required double-pulse resolution,

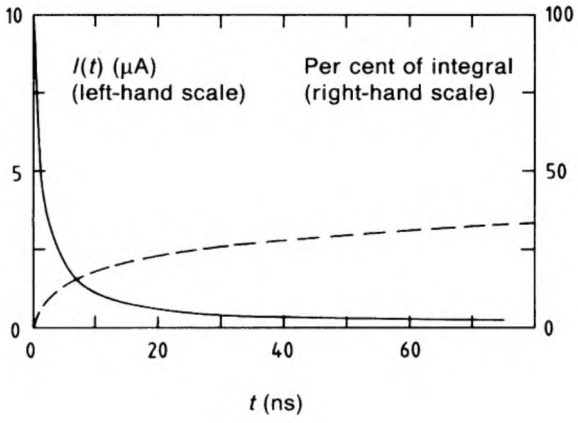


Figure 3.3: Current signal according to Eq. 3.5 (full line, left-hand scale) for t_0 = 1.25 ns, b/a = 500, and $N_{tot} = 10^6$ elementary charges. Time integral Eq. 3.6 of this pulse as a percentage of the total charge (broken line, right-hand scale) [24].

signal occupancy, gain and baseline uniformity. This requirement justifies the need for an ion tail-cancellation (TC) component in the ASIC circuitry.

3.2 PASTTREC

The PASTTREC ($\overline{\text{P}}$ANDA Straw Tube Tracker REadout Chip) is an 8-channel straw tube read-out Application Specific Integrated Circuit (ASIC) for the $\overline{\text{P}}$ANDA experiment. The time-sensitive architecture of the PASTTREC FEB is designed using the 0.35 μm CMOS technology by D. Przyborowski from AGH [2, 21], fulfils all the requirements defined in Section 3.1 to read-out the straw tubes.

3.2.1 Analog

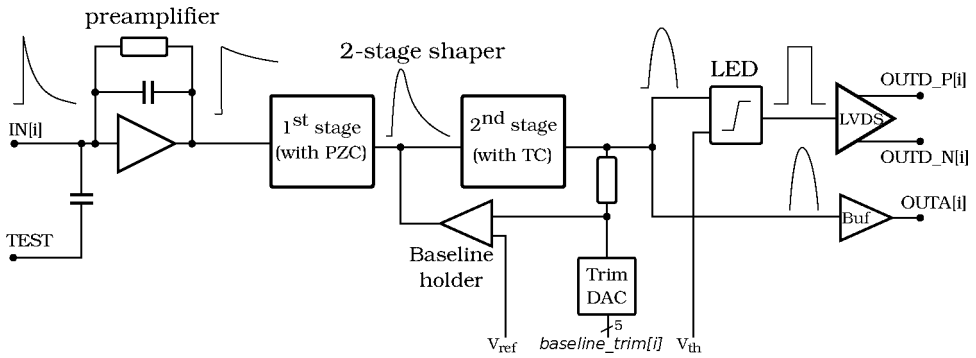


Figure 3.4: Block diagram of an 'i^{th}' ASIC channel consisting of Charge Sensitive Pre-amplifier (CSP), Pole Zero Cancellation (PZC), two-stage tail cancellation circuit, Base Line Holder (BLH), Leading Edge Discriminator (LED), and LVDS output [21].

Each PASTTREC channel comprises a Charge Sensitive Pre-amplifier (CSP) with a variable gain and a discharge time constant, a Pole Zero Cancellation (PZC) unit, a second order shaper with a variable peaking-time, an ion tail cancellation

circuit with trimming, a BaseLine Holder (BLH) to stabilise the baseline, a Leading Edge Discriminator (LED) with Low Voltage Differential Signalling (LVDS) output, and a buffered analogue output. The block diagram of the designed read-out for a single channel is shown in Figure 3.4. The CSP, low pass and high pass filters (CR-RC circuit) perform the first stage of signal shaping, and the PZC eliminates the signal undershoot originating from the CR-RC part. The second stage shaper has a configurable CR-RC tail suppression circuit (TC) that approximates the signals with different amplitudes and time constants. If the baseline level is shifted, measured lead-time and TOT would be incorrect. For this purpose, the BLH in the PASTTREC allows setting the baseline level to the FEB channels individually. The shaped signal is discriminated at the LED, and the time of arrival of the signal and the TOT is extracted. The digital output signal of the LVDS standard is produced when the analogue signal level overpasses the discriminator threshold. The specifications of the designed PASTTREC are listed in Table 3.3. The first version of the PASTTREC FEB was developed in 2011, and since then, it has undergone continuous improvements; at the moment, we have the fourth version of the FEB. The current version is more energy efficient, smaller and includes additional features that will be discussed further. Two such PASTTREC chips were packed on a Printed Circuit Board (PCB), and the photograph of the ASIC and the FEB is shown in Figure 3.5.

Table 3.3: Main parameters of PASTTREC

Technology	0.35 μm CMOS
Number of channels	8
Equivalent (delta) input range	0-200 fC
Variable gain	~0.67-4 mV/fC
Variable peaking-time	10-35 ns
Noise ENC	<1 fC
Baseline tuning	-30 - 30 mV
Signal Input	single ended
Output standard	LVDS
Power consumption	~ 35 mW/channel
Control interface	SPI

3.2.2 Digital

PASTTREC is a highly configurable ASIC with 64k possible settings that include pre-amplifier gain, peaking-time, tail cancellation, signal shaping parameters and digital-to-analogue converter (DAC) for the baseline and threshold settings. They not only allow us to optimise the chip's performance for the working conditions of the straws but also allow the chip to be used in other applications where high accuracy of time measurement is required in high counting rate environments. Table 3.4 presents a list of these parameters, ranges and regulations.

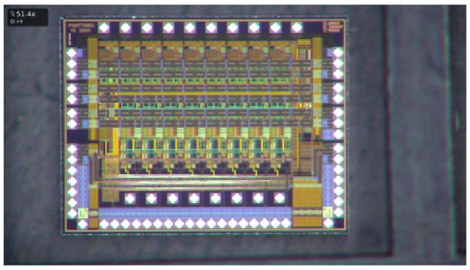


Figure 3.5: Left: A magnified Photograph of the PASTTREC ASIC. Right: A 16-channel FEB for the $\overline{\text{P}}$ANDA FT mounted with two PASTTREC ASICs (covered by an aluminium shield).

Table 3.4: Available PASTTREC settings

Parameter	Values
Gain (K)	0.67,1,2,4 mV/fC
peaking-time (Tp)	10,15,20,35 ns
1^st stage tail cancellation capacitance	1-16.5 pF (step 1.5 pF)
1^st stage tail cancellation resistance	$\sim$ 3-31 kΩ (step 4 kΩ)
2^nd stage tail cancellation capacitance	0.6-1.65 pF (step 0.15 pF)
2^nd stage tail cancellation resistance	5-26 kΩ (step 3 kΩ)
Common discrimination threshold	0-254 mV (step 2 mV)
Baseline fine-tuning	-31 to +31 mV (step 2 mV)

PASTTREC Registers

The FEB for straw tubes has a digital module for slow control communication. It has a set of 8 bits registers which can configure the PASTTREC behaviour. The description of all 14 registers can be found in Table 3.5. The 'x' symbol indicates not the important bit. The baseline for the PASTTREC channels in the BLH can be set either from the 1V band-gap circuit or externally from the pad by changing the value of Bg_{int} register (1- internal, 0 - external). Register K_0 and K_1 change the field gain of the CSP ('b00 - 4 mV/fC, 'b01 - 2 mV/fC, 'b10 - 1 mV/fC, 'b11 - 0.67 mV/fC). The peaking-time of the signal can be changed used the Tp_1 and Tp_2 registers ('b00 - 10 ns, 'b01 - 15 ns, 'b10 - 20 ns, 'b11 - 35 ns). The register values for setting the CR-RC tail-suppression and shaping circuit are described in Table 3.6 by reg_1 and reg_2. The LED threshold has six registers that define what is common for all the channels. The value changes the threshold with respect to baseline value V_{ref}, from V_{ref} to V_{ref} + 254 mV in steps of 2 mV. The baseline position can be controlled using the 5-bit Bl registers from V_{ref} = -32 mV to +32 mV in steps of 2 mV. Register 12 disables (0) or enables channels and LVDS outputs, and register 13 controls the LVDS current. The last register controls LVDS current. All the registers in the PASTTREC can be set with a value and read-back using the Slow Control module, which is further described.

Table 3.5: Description of the PASTTREC registers

	Registers	Bits (MSB → LSB)							
1	reg_0	x	x	x	Bg_{int}	K_1	K_0	Tp_1	Tp_0
2	reg_1	x	x	TC_1C_2	TC_1C_1	TC_1C_0	TC_1R_2	TC_1R_1	TC_1R_0
3	reg_2	x	x	TC_2C_2	TC_2C_1	TC_2C_0	TC_2R_2	TC_2R_1	TC_2R_0
4	reg_3	x	V_{th6}	V_{th5}	V_{th4}	V_{th3}	V_{th2}	V_{th1}	V_{th0}
5	reg_4_11	x	x	x	Bl_4	Bl_3	Bl_2	Bl_1	Bl_0
6	reg_12	x	x	Ch_2	Ch_1	Ch_0	$LVDS_2$	$LVDS_1$	$LVDS_0$
7	reg_13	x	x	x	x	x	$LVDS_2$	$LVDS_1$	$LVDS_0$

Table 3.6: Tail Cancellation register values.

Value	TC_1C	TC_1R	TC_2C	TC_2R
'b000	6.0 pF	3 kΩ	0.60 pF	5 kΩ
'b001	7.5 pF	7 kΩ	0.75 pF	8 kΩ
'b010	9.0 pF	11 kΩ	0.90 pF	11 kΩ
'b011	10.5 pF	15 kΩ	1.05 pF	14 kΩ
'b100	12.0 pF	19 kΩ	1.20 pF	17 kΩ
'b101	13.5 pF	23 kΩ	1.35 pF	20 kΩ
'b110	15.0 pF	27 kΩ	1.50 pF	23 kΩ
'b111	16.5 pF	31 kΩ	1.65 pF	26 kΩ

3.2.3 PASTTREC FEB Characteristics

PASTTREC chips (2 on each FEB) were bonded to a dedicated printed circuit board (PCB) of the size 5.3 × 8.6 cm, as shown in Figure 3.5. Four-layer PCB has 16 input and 16 differential (LVDS) output lines transmitting the leading edge discriminator outputs for the timing measurements. An alternative PCB board with additional analogue buffers, driving signals from 16 channels via MMCX connectors, was developed for the inspection of analogue signals. This board was used for measurements of signal shape, front-end gain, noise distribution etc. Figure 3.6 shows the analogue output of the PASTTREC for three different TC settings at CSP gain K=1 mV/fC and the peaking-time PT = 20ns. The analogue signals have no significant undershoot nor overshoot, an amplitude high enough to be discriminated early for various possible pulse time duration. The parameter setting with the best time and position resolution has to be determined and will be discussed in detail further in Section 3.4.4. The basic characteristics of PASTTREC signals have been studied in the past and described in detail in [3].

The PASTTREC channels also have low noise and gain uniformity. Indeed, the measured spread of the CSP gain coefficient of 1.3% is very good and is considered sufficient for treating all straw channels as having equal gain without further TOT calibration, provided that baseline levels for all channels. Figure 3.7 (Left) shows the correlation between the input charge and the output amplitude for 16 PASTTREC channels. This also justifies a common threshold approach and guarantees that timing information obtained from the leading edge discriminator, measuring the time of the signal crossing the threshold, is not biased by different baseline positions of various channels. The chip performance measurements have shown [21], the time jitter of a single channel amounts only to 0.14 ns, which is good enough for drift-time

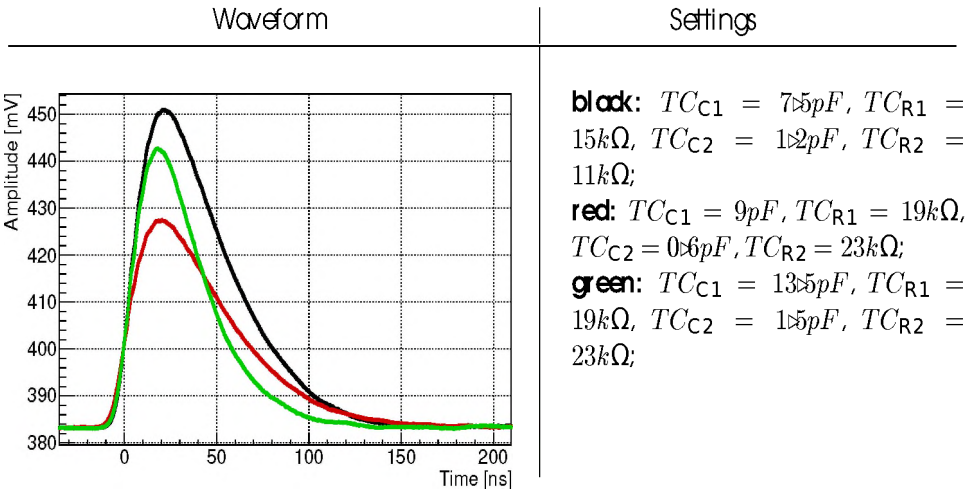


Figure 3.6: Analog output for three different TC settings found for the pre-amplifier gain K=1 mV/fC and the peaking-time PT=20ns [3].

calculation. The relation between input charge and output amplitude is linear in the measurement range of the $\overline{\text{P}}$ANDA FT straws for all the CSP gain (K) settings as seen in Figure 3.7 (Right). The PASTTREC chip also has the capability to process hit rates reaching up to 1-2 million per second the maximum rate that FT straws will experience at $\overline{\text{P}}$ANDA. The pulse of 2 MHz frequency has been directed to the chip, and the result of the analogue output is presented in Figure 3.8. This uniform distribution also demonstrates the stability in the baseline position at high hit rates. These results were obtained by connecting two test inputs to PASTTREC FEB pads dedicated for charge injection to the chip via internal capacitors to measure the response to a δ-current source. 16 LVDS signals are transmitted via KEL 8930E 40-pin connector, which provides 4 additional LVDS lines for the ASIC parameter setting. The FEBs are connected to the straw tubes via an additional passive resistor-capacitor (RC) board equipped with resistors for limiting the straw-wire current and capacitors for voltage decoupling.

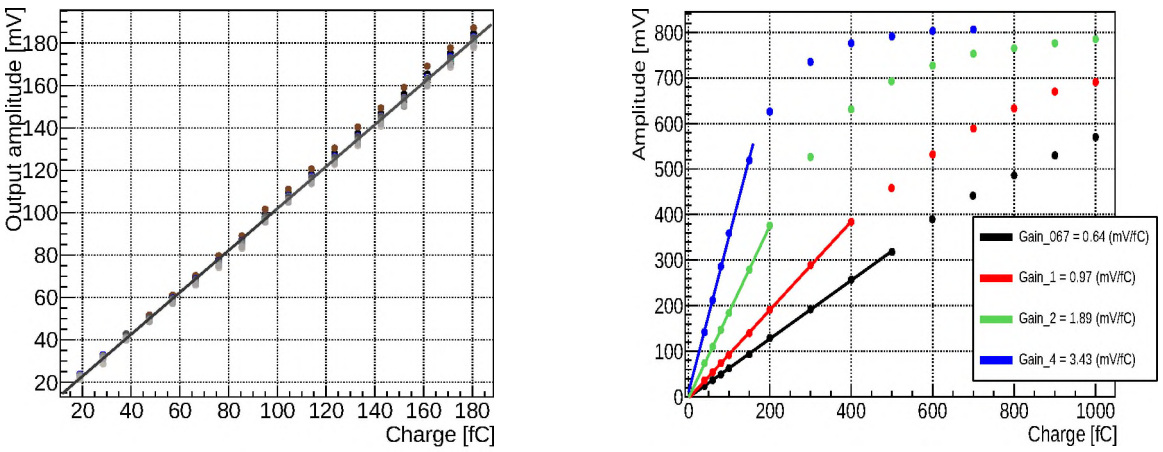


Figure 3.7: Left: Gain functions for δ pulses for the four CSP gain parameter (K) settings for a known TC setting. Right: Amplitudes of 16 output signals versus input charge for the same ASIC configuration [3].

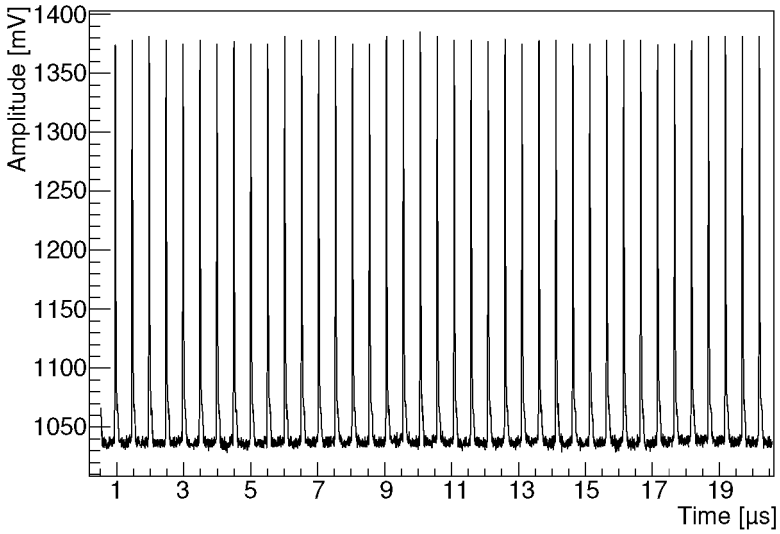


Figure 3.8: The analogue output of the PASTTREC chip responding to the pulse coupled to the FEB test input. The input pulse frequency equals 2 MHz [3].

3.3 Slow-Control

The Front End Board contains two PASTTREC ASICs that share a common set of Slow-Control lines, that is provided through a connection to an external FPGA. The lines consist of the following: SDO, SDI, CS, and SCK in the LVDS25 electrical standard as shown in Figure 3.9. These lines are distributed from the connector to both the ASICs; therefore, the selection of active PASTTREC has to be done through a dedicated header bit in the transmitted data.

The digital part of the PASTTREC ASIC responsible for the Slow-Control has been designed to operate at clock rates up to 25 MHz. However, to make the transmission less noise prone, a lower frequency has been used (96 kHz). The registration of the incoming bits through the serial data line (SDO) is activated at the rising edge of the serial clock (SCK). The protocol is similar to the Serial Protocol Interface (SPI) except for the chip select (CS) line purpose, which is used as a reset for both of them instead of activating a particular chip. At the very beginning, before issuing any slow-control command chip should be reset because there is no power-on reset in the ASIC. Reset sets all internal registers to their default values. The reset signal is active low and synchronous, and therefore clock signal has to be active during the whole reset sequence. It may last any number (at least one) of clock cycles, but when removed during the next 5 cycles, the chip is still internally reset, so the user should wait for at least 6 cycles before sending any command. When the reset is done, the chip can be programmed by slow-control commands, which have to fulfil a particular format as described below:

```
Header[3:0]|Address[1:0]|R/W|RegNo[3:0]|RegData[7:0]
```

The *Header* is constant and must be ‘b1010. The command is executed only if the value in field *Address* is equal to the chip ID. The PASTTREC waits for a header only when the previous command was ended regardless of received *Address*. The PASTTREC receiving correct *Address* sends the value of register *RegNo* as described in Table 3.5 through the output line SOUT. If the bit *R/W* is zero, then

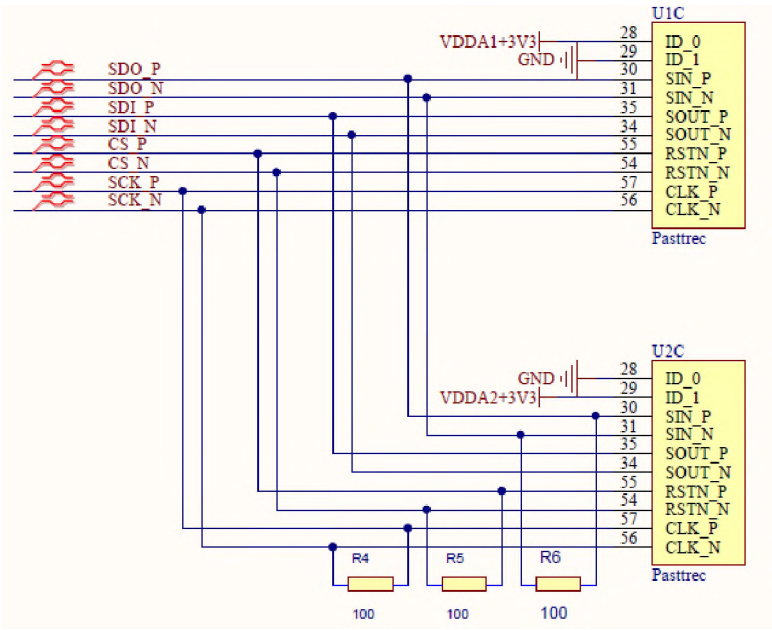


Figure 3.9: Schematics of the FEB with two PASTTREC devices and interface ports for slow-control.

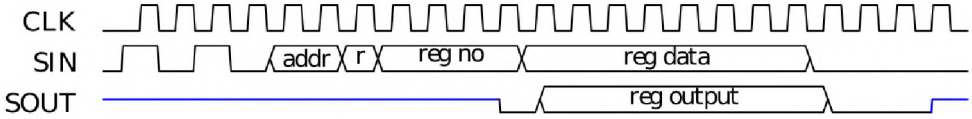


Figure 3.10: PASTTREC Slow-Control Data Format.

the register *RegNo* is written with the new value *RegData*, as described in Table 3.7. In the opposite case (bit *R/W* is one), the chip only sends out the current register value. Output SOUT is always in the high impedance state except when the chip is transmitting data. The data buffer at SOUT is turned on when the last bit of *RegNo* is sampled. The first bit sent by the buffer is zero and should be ignored. This clock cycle gives the output LVDS time to start avoiding data distortion. Then, register contents are sent (8 bits), and the buffer is still active during the subsequent three clock cycles. As a result, to ensure the buffer is off, at least five zeros should follow the register data (*RegData*). The timing diagram of the command is shown in Figure 3.10. In order to verify the transmission, read-back of the registers from the PASTTREC to the FPGA must also be assured through the SDI line. Considering all clock cycles necessary to deactivate output buffers, a single command is 23 bits long. However, if many commands have to be sent sequentially, they might be partially pipe-lined.

3.3.1 Communication Protocol

In the case of PASTTREC ASIC, the Slow Control functionality is limited to read and write operations performed using an interface and a protocol similar to a Serial Peripheral Interface (SPI). All operations originate from the user who issues a particular command from a PC connected via the network to the FPGA on the TRB. The firmware in the FPGA contains a component responsible for decoding commands and the transmission to the selected FEB and PASTTREC ASIC.

An SPI controller component is developed especially for PASTTREC-based FEBs and is part of the TRB firmware and software package. A single 32-bit word containing appropriate addresses, registers and values is delivered to the component, which extracts the fragments dedicated to PASTTREC and initiates serial transmission of the bits to the device.

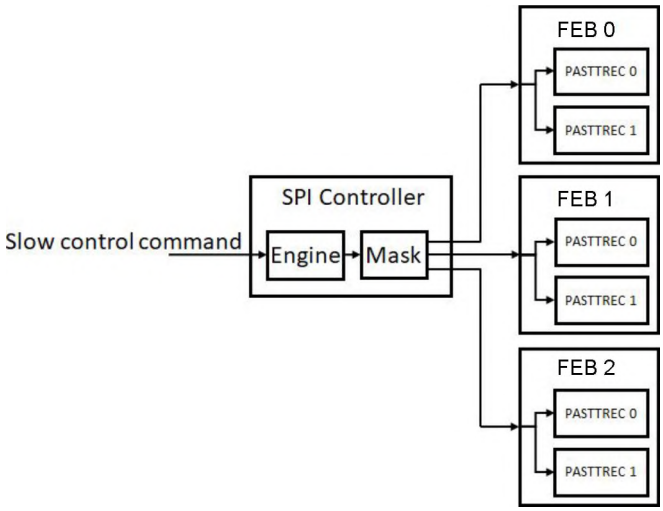


Figure 3.11: Schematics of the connectivity between the SPI controller and FEBs with PASTTREC ASICs.

The FPGA can control a pre-defined number of FEBs having two PASTTREC ASICs, see Figure 3.11. In order to address a particular PASTTREC on a FEB, additional two bits must precede the actual data word (bits 14-13, described in Table 3.3). The firmware contains one SPI controller and 3 sets of dedicated lines to the FEBs. By default, the commands are distributed to all connected boards. In order to select an active one (the CS-chip select line is used for the reset), one has to disable the others by masking the outgoing SCK and SDO lines using dedicated control registers. Sending a command to PASTTREC consists of two steps: (i) setting the command bits by writing a register and then (ii) launching the transmission to the ASIC by activating a bit in the SPI controller. In the case of the register read command, the appropriate command has to be sent (bit 12 in the command data word) that retrieves the PASTTREC register value back and stores it in a dedicated FPGA register of the SPI controller (0xD412 on Table 3.7). Resetting the ASIC requires activating the chip select (CS) bit for at least 25 clock cycles. Table 3.7 contains the SPI controller registers for PASTTREC. For the management of the PASTTREC (write, read, reset etc.), a web tool based on Perl, JavaScript and CSS is used.

3.4 Qualification of PASTTREC FEBs

The $\overline{\text{P}}$ANDA FT is a large detector with over 12 thousand straws using over 1500 PASTTREC ASICs. Production of FEB, including PASTTREC, is a part of the in-kind contribution to the FAIR project realized by AGH and JU (AGH is a leading Institution). It is essential to show that all PASTTREC channels have optimum performance. The parameters for the successful operation of PASTTRECs have

Table 3.7: SPI controller registers

Address	Description
0xD400	Command data word
0xD411	Launch serial data transmission
0xD412	Register readout value
0xD415	Disable (b1) SDO output lines (bit index is the connector index)
0xD416	Disable (b1) SCK output lines (bit index is the connector index)
0xD417	Disable (b1) CS output lines (bit index is the connector index)

been defined and verified by us in the dedicated test procedures. These parameters include the health of the PASTTREC channels, uniformity and stability, electronic noise levels, the power consumption etc, as described in detail below.

3.4.1 Measurement tools and techniques

Two of the most important parameters of the PASTTREC are gain and baseline uniformity. High gain uniformity of the PASTTREC allows treating all the channels equally, without requiring individual calibration procedures for leading-time and TOT measurements. However, baseline levels of all channels, which differ due to the complex manufacturing process, must be aligned after power-up. This can be achieved, thanks to an internal DAC circuit which allows changing individual baseline-threshold levels to be located in the middle of the noise band measured for each channel separately. The intensity of the noise and its relative distance to the threshold at the 0 mV position allows for determining a particular channel's suitability for operation. To find such baseline positions, two methods have been investigated: S-curve measurement and the noise profile scan. During both procedures, the baseline or threshold of each channel in the chip is shifted, and the number of registered output pulses is measured at each step. What differs between the methods is the source of the input signal: in the S-curve measurement, an external pulse generator is required, while in the noise profile method, only the noise of a channel is measured (with a detector connected to FEB). In both methods, the number of counts as a function of the baseline/threshold position is determined and further analysed to extract the qualification values. These two methods are further described.

S-Curve

The PASTTREC channels are injected with signals of fixed amplitude at a constant frequency, the discriminator threshold is varied in steps, and the counts at the output of the discriminator are registered. Ideally, the hit occupancy would follow a step distribution, but the distribution is smeared by the electronic noise. Figure 3.12. illustrates normalised counts while injecting the test signals convoluted with a Gaussian-distributed electronic noise. Assuming the input signal distribution is described by a Gaussian probability distribution function S (x$\prime$). The noise width

is then calculated after fitting the count profile with the error function:

$$S(x\prime) = \int_{-\infty}^{x\prime} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2} dx = A\frac{1}{2}[1 + erf(\frac{x\prime - \mu}{\sqrt{2}\sigma})] \tag{3.7}$$

Where A is the number of test pulses, $x\prime$ is the threshold level, μ is the mean signal amplitude (denoted as vt_{50} in Figure 3.12) and erfc is the complementary error function. The width of the distribution gives a measurement of the noise amplitude at the discriminator output. For standard analysis, the input threshold difference between 84% and 16% is taken as counts corresponding to 2σ.

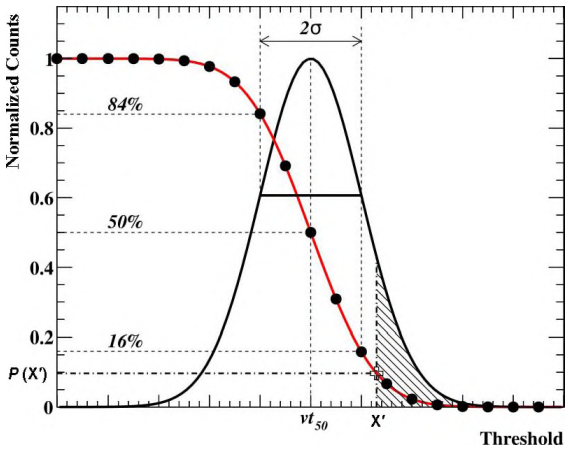


Figure 3.12: A schematic representation of the s-curve scan. The threshold x$\prime$ is varied in steps, and a test pulse is injected a certain number of times at each threshold point. The total input signal results from the convolution of the calibration pulse and some electronic noise described by a Gaussian distribution function. For a given threshold x$\prime$, the count rate corresponds to the fraction of signals above the threshold (dashed area) [25].

Noise profile scan

In order to measure the baseline position for each channel in the chip, without the usage of an external pulse generator, a dedicated fast procedure called noise profile scan was developed. This procedure was later a standard automatic tool used for baseline settings of PASTTRECs in the beam operation of the detector. In this procedure, FEB is connected to straws and a common threshold value of 0 mV is set. The baseline positions for each chip channel are varied within the allowed range of -30 to +30 mV with a 2 mV step. During the scan, the number of counts is measured for each baseline position and every channel. The baseline position is determined from the measured profile of the number of counts as its mean value as given by Eq. 3.8.

$$MeanBaselinePosition = \frac{\Sigma B_{imV} C_i}{\Sigma C_i} \tag{3.8}$$

Where, B_i is the baseline at position i, C_i is the counts registered for baseline B_i and $B_{imV} = (B_i \times 2)$ - 32 (conversion from DAC LSB to mV). The calculated mean value is subtracted for each channel by the respective DAC setting as shown

in Figure 3.13. The measured signal count profile has approximately a Gaussian shape. It is used to characterise the noise of individual channels by means of RMS. This scan method is very useful for simultaneously measuring baseline position and noise width from a large number of FEBs.

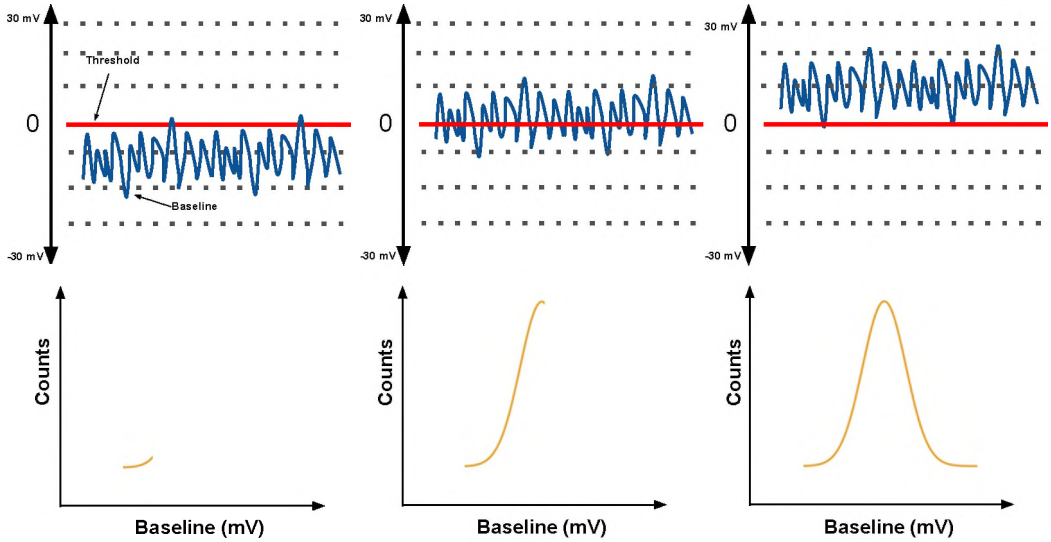


Figure 3.13: Representation of the signal count as a function of the baseline position at various stages of the baseline scan

The noise level is another important characteristic of the chip's performance since it determines the lowest possible threshold setting. As mentioned above, the low threshold position w.r.t baseline is essential for improved detector performance. It needs very careful consideration as it influences the efficiency and count rates of the detector.

3.4.2 Noise, Baseline and TOT

In order to study the electronic noise in the PASTTREC channels, both the s-curve and noise profile methods were compared. A pulse generator was used, and test pulses of amplitude 120 mV were injected at 1 MHz frequency into the inputs of PASTTREC FEB channels connected to the detector module. As the PASTTREC allows for the change in baseline position, the baseline is shifted from -30 mV to +30 mV in 2 mV steps, and the counts are recorded. The profile is fitted with the error function as described in Eq. 3.7 and the obtained parameters p0 (counts), p1 (mean) and p2 (σ of noise width) are presented in Figure 3.14. The disadvantage of this method is that it takes a significant amount of time to complete the scan and it requires externally generated pulsed. The latter practically eliminates it from the in-beam application. We are limited by the number of channels in the pulse generator used for charge injection and cannot simultaneously scan FEBs when FEBs are mounted on the full-scale detector.

In the next step, the noise scan is performed for the same PASTTREC FEB channel, and the count profile is presented in Figure 3.14. The resolution of the scan steps is limited by the DAC LSB, i.e. 2mV. As the internal PASTTREC noise is very low (<1 mV), the noise scan has to be performed at the highest CSP gain (4 mV/fC). This way, the noise is amplified and has a better chance to be captured

by the scan. The σ of the normal fit on the count profile represents the width of noise in the channel. The σ of noise scales linearly with the gain; hence for the 1 mV/fC, it is factor 4 smaller than for 4 mV/fC. Additionally, to also capture the real-case situation, the scans are performed with the PASTTRECs connected to the detector (n.b reduction of this noise is an important aspect related to the electrical fluctuations and grounding scheme of the detector and electronics).

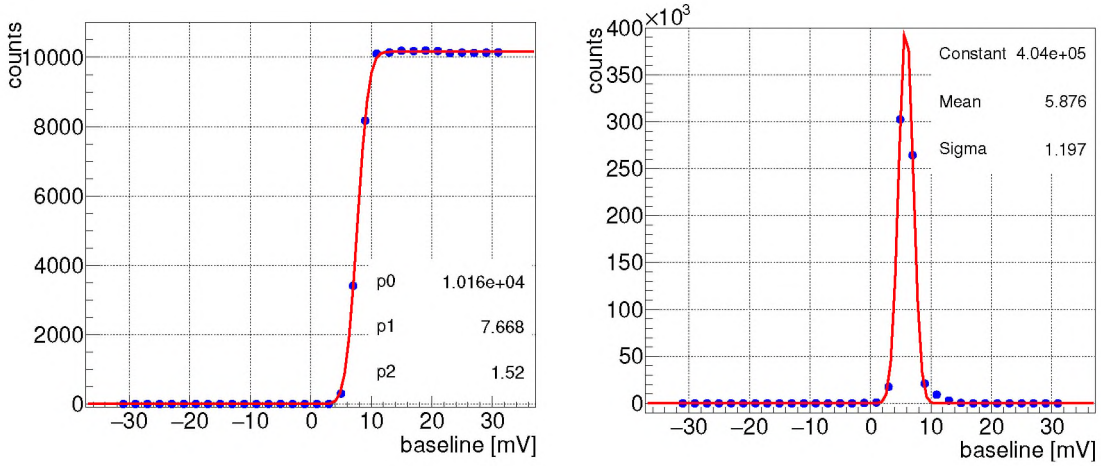


Figure 3.14: Left: Signal counts at the digital output obtained from the S-curve measurements of a PASTTREC channel. The counts (blue points) are measured as a function of baseline level scan fit with error function (red line) for a PASTTREC channel. Right: Signal counts as a function of baseline position for a PASTTREC channel (blue points) fit with a normal distribution (red line).

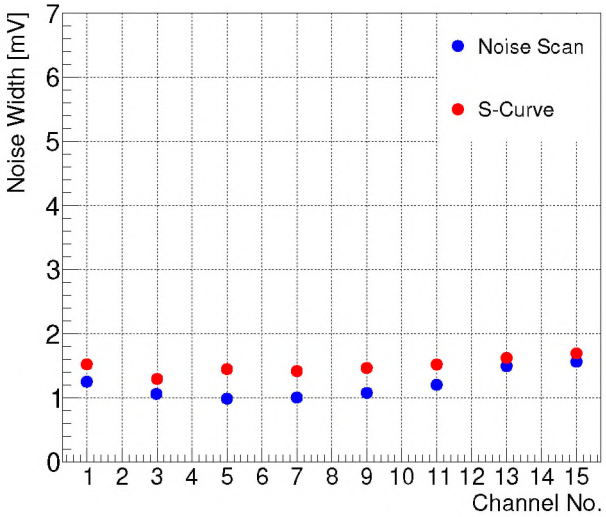


Figure 3.15: Comparison of the noise width (σ) from the two methods shown on the example of one FEB.

Regarding the noise, the comparison of the two methods on an example of one board is gathered in Figure 3.15. The same FEB was scanned twice, once with the S-curve measurement and then with the noise profile method. Although the

absolute values of the σ calculated with S-curve measurement are systematically higher, the relations between the channels are consistent enough to use the noise profile method as a reliable measurement for the qualification of the boards. Very precise noise measurement is not the primary goal of this work, as the noise is not high (the typical amplitude for MIP amounts to ≈150 mV at CSP gain 1mV/fC or ≈650 mV at CSP gain 4mV/fC). Hence, there is a large margin for setting the discriminator threshold without affecting the detection efficiency. Moreover, the noise profile method represents the true operational environment (FEB connected to the detector), and it has a few practical advantages: The measurement can be performed automatically and remotely for any number of FEBs, without the need for reconnecting an external pulse generator. In fact, this method has been verified to qualify FEBs for setups with many detector modules, and the results from in-beam measurements fully confirmed its usefulness.

The final verification of the baseline alignment is made by means of radioactive sources (or beam particles in in-beam operation). PASTTREC FEBs are connected to the detector which is irradiated with a radioactive source of known energy. TOT distributions are measured for channels, and the baseline positions are inspected. The distortions or shifts in the TOT distribution are mainly caused by non-uniform baselines in the PASTTRECs. In cases where some shifts are observed baseline positions are to be fine-tuned in steps until all the channels obtain the same TOT value. This is a very time-consuming procedure and requires the detector to be operational. For this reason, instead of manually tuning the baselines based on TOT values, the mean position of the baseline obtained from the noise scan (as described in Section 3.4.1) is used to calculate the offset in the baseline position. This offset is later used to align the baselines to have a common TOT.

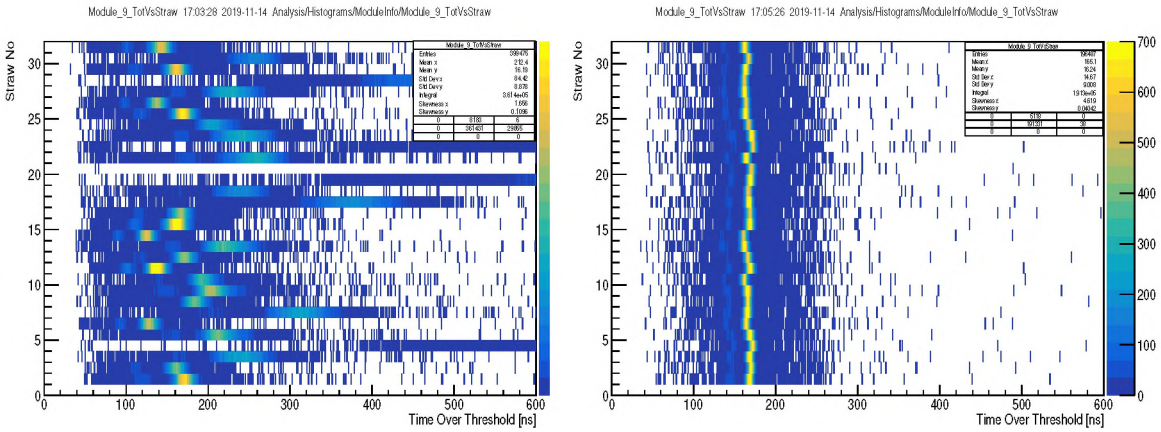


Figure 3.16: time over threshold accumulated from 16 channels by irradiating the straws with ^{55}Fe radioactive source Left: After setting all the baselines to a common value of 6mV, Right: After the automatic alignment of the baseline position. The slight non-uniformity observed here is due to partially due to the non-uniformity in straw gains.

The effect of the alignment procedure can be visualised by inspection of uniformity of the Time Over Threshold (TOT) distribution for the straw channels irradiated by ^{55}Fe X-ray source. A typical example for one straw module (32 channels) is shown in Figure 3.16 - before (left) and after the automatic alignment procedure (right). The relation between the baseline level of a particular channel and

the common discrimination threshold level corresponds to a TOT value for a given input signal amplitude. As one can see the effect of baseline alignment is significant. Without it a common threshold effectively discriminates the input signal at different levels; therefore, the TOT value differs. After the baseline alignment, all channels discriminate the input signals at the same levels, resulting in uniform TOT measurements. The final effect of TOT uniformity can also be appreciated on one-dimensional projection presented in Figure 3.17.

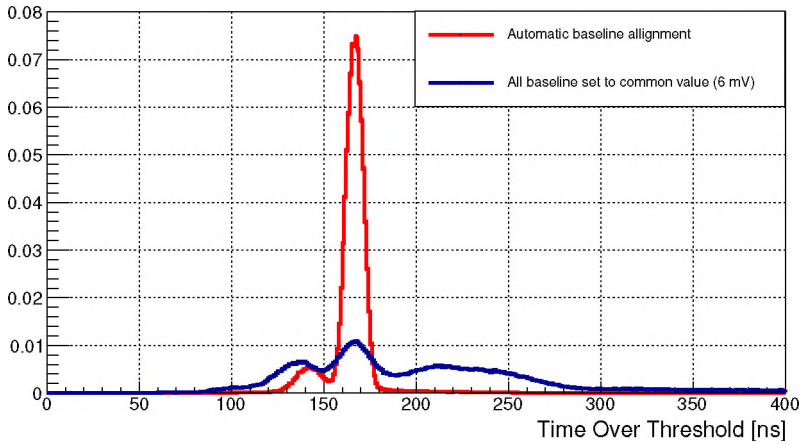


Figure 3.17: Time over Threshold accumulated from 32 channels by irradiating the straws with ^{55}Fe radioactive source. Blue: After setting all the baselines to a common value of 6 mV, Red: After the automatic alignment of the baseline position using the noise-scan procedure.

The distribution obtained after setting all the baselines to a common is very broad, while the one obtained after the alignment of the baseline positions is narrow and reveals a 5.9 keV line (a satellite peak at lower TOT is an Ar-escape peak).

As described earlier, during the scan, the number of counts is measured for each baseline position and every channel. The baseline position is determined from the measured profile of the number of counts as its mean value. The calculated mean value is subtracted for each channel by the respective DAC setting. The baseline position is an intrinsic property of the PASTTREC channel and is expected to remain constant at all conditions, irrespective of the ASIC setting. It was verified that the obtained baseline position does not depend on peaking-time and TC settings configured to the PASTTREC and is presented in Figure 3.18. This implies that once the baseline positions are determined, the offsets calculated can be used to align the baseline positions to a common value irrespective of the detector and PASTTREC operating conditions. This is an important result because it means that once baseline positions are determined, they can be stored in a database and applied anytime during the beam operations in the experiment.

All the results from the noise profile scans are later used for the statistical analysis of the FEBs. These measurements described above are performed with the dedicated system and are controlled by specially prepared software. The components of this system are described in more detail below.

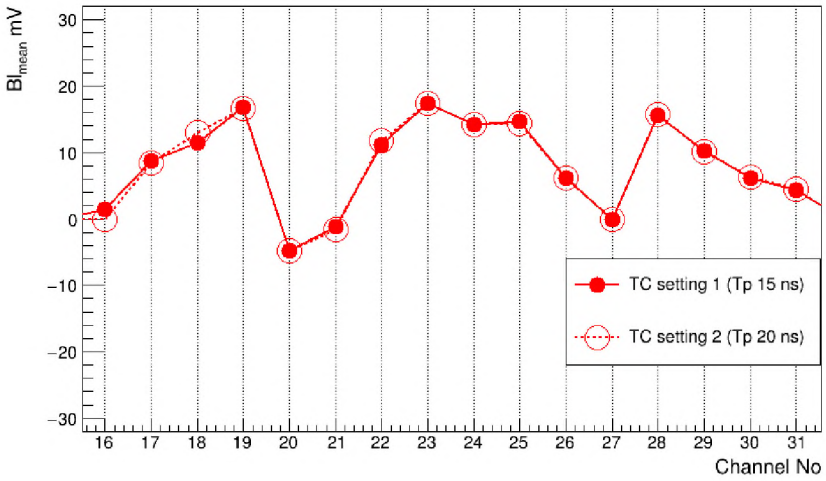


Figure 3.18: Baseline positions determined by the noise-scan procedure of 16 channels from one FEB (2 PASTTREC chips) connected to the straw detector configured with two different settings. TC setting 1: K=4 mV/fC, Tp=15 ns, TC_1C=9 pF, TC_1R=19 kΩ, TC_2C=0.6 pF, TC_2R =23 kΩ. TC setting 2: K=4 mV/fC, Tp=20 ns, TC_1C=10.5 pF, TC_1R=27 kΩ, TC_2C=0.9 pF, TC_2R=20 kΩ.

Software Tools

TrbNet is a communication protocol developed for transporting data from the custom FEB to the FPGA in the TRB. A software based on the TrbNet binding was developed using python3 for the complete management of the PASTTREC FEBs. This means the PASTTREC configurations can be controlled, and the data (counts rates, lead-time, TOT) can be gathered. This tool includes measurement, analysis, and visualisation modules for the noise profile scan and baseline alignment of the PASTTREC channels. Some of the most important functionalities of this software are listed below.

- asic_read: Read values from any PASTTREC register described in Table Table 3.5.
- asic_reset: The PASTTREC has to be reset after power-up as described in Section 3.3.
- asic_set_reg: Write values to any PASTTREC registers. For Example, to control the CSP gain, TC setting etc.
- asic_threshold: Allows for adjusting the discriminator threshold levels.
- baseline_calc: Calculate the baseline position from the scan outputs.
- baseline_merge: Merge the outputs of the baseline-noise scan from multiple PASTTREC FEBs into a single file. This can be later used to upload the aligned baseline positions to all the FEBs at once.
- baseline_scan: Performs the noise profile scan by setting the threshold to 0 mV and gathering the counts for every step increase in baseline position. This can

be performed for all the PASTTREC channels in the system at the same time or on one channel of each PASTTREC at once. In the latter case, electronic cross-talk can be avoided during the scan and is the [preferred option.

- communication_test: It is important to confirm the communication with all the PASTTREC registers in their respective channels after every reset. This is ensured by writing and reading to some registers in the PASTTREC channels.
- draw_baseline_scan: The count profile from the noise scan is plotted for every channel.
- scalers_scan: Gather the count rates or total counts from all the PASTTREC channels at defined intervals.
- threshold_scan: Unlike baseline scan, where the threshold is set to a constant and the baselines are scanned, the procedure can also be applied vice-versa by setting the baselines to a constant value for all the channels and scanning the threshold. The results of the scan should be compatible.

The software can be downloaded from url: pasttrectools.

Power consummation

The maximal power consumption of the FEB is 56 mW/channel with a supply voltage of 5V -see Figure 3.19. The nominal supply voltage of the PASTTREC is 3.3 V which is assured by at least 3.5 V supplied to the voltage regulator placed on the FEB card. It corresponds to the nominal power of 40 mW/channel while the power consumption of the PASTTREC remains stable irrespective of the ASIC setting. All FEB boards should consume the same amount of power in an idle state, which is the first criterion to qualify the FEB board for future use. PASTTRECs will also be used in the Straw Tube Trackers (STT) in the $\overline{\text{P}}$ANDA central tracker, which is comparatively a more compact system with limited space for airflow and heat dissipation. The power consumption and heat dissipation in PASTTRECs has to be under acceptable limits for STT.

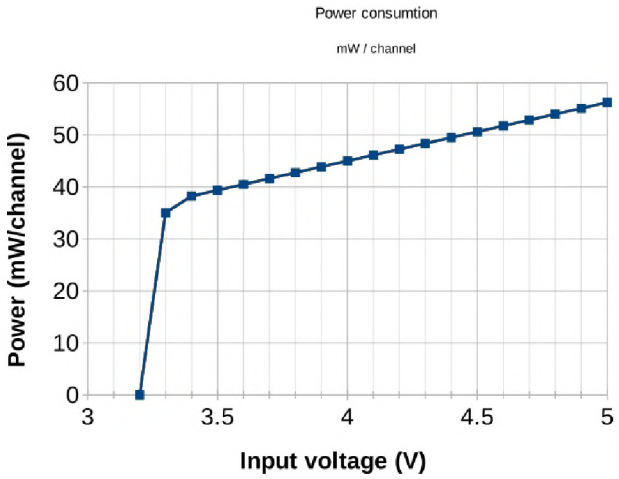


Figure 3.19: Power consumption per PASTTREC channel as a function of input voltage showing a constant power utilisation between 3 - 5V.

3.4.3 Qualification scheme

All produced FEB cards must be qualified before being accepted for operation in the final read-out system. First, an optical inspection of the FEB assembly quality is done. Later, each board acquires a unique identification number, and some qualification measurements are performed. Lowering the discriminator threshold will significantly improve the time resolution of the detector signals while providing the opportunity to lower the operational detector voltage, thus reducing the ageing of the detector. The acceptance criterion is to have the noise width (σ) less than five sigmas below the operational discriminator threshold (i.e. lesser or equivalent to 6 mV at a gain of 1 mV/fC). With this objective, all the FEBs will be tested and qualified based on their quality into the groups described below. The main results: power consumption of the FEB and the baseline levels, and noise sigma for each channel, will be stored in a database for future use and reference.

- Green : Power consumption is in the range of 55 mW/channel ±15 % at 5V supply voltage (PASTTREC power approximately 40 mW/channel ±15 %). At pre-amplifier gain 4mV/fC and Tp=20 ns, noise σ is at least five times lower than the discriminator threshold 24 mV. The gain of 1mV/fC corresponds to σ five times lower than 6 mV. Baseline positions allow aligning all channels to a uniform discrimination level (verified by measurement with an external signal source, e.g. with the detector and ^{55}Fe source). Board is ready to be used in the system.

- Blue : Power consumption is in the range of 55 mW/channel ±15 % at 5V input voltage (PASTTREC power approximately 40 mW/channel ±15 %). Maximum one channel does not fulfil the noise and baseline levels specifications from the Green category. A detailed description of the FEB malfunctioning is archived. Usable in regions of the detector where not all channels are connected to the detector.

- Red: FEB does not fulfil categories Green or Blue specifications. A detailed description of the FEB malfunctioning is archived. If necessary, such FEB requires inspection or repair.

3.4.4 Optimal Settings

The qualification parameter ensures the quality of the PASTTREC channels and stable performance under all operational configurations. CSP gain, peaking-time, tail cancellation, shaper circuits and DACs for baseline settings and a discriminator threshold are the configurable parameters of PASTTREC. It is up to us to evaluate and choose the configuration suitable for the application. All the configurations with the lowest peaking-time (10 ns) were eliminated due to the pickup noise in the straws. Furthermore, the lowest amplification (0.67 mV/fC) was eliminated as it would require higher voltage in the straw tubes, which is not optimal from the point of view of the detector ageing effect. All the remaining configurations with the gain (1,2,4 mV/fC) and peaking-time (15,20,35 ns) were carefully studied and well described in the past by Dr Paweł Strzempek in his PhD thesis [3]. TC parameters were defined for each of the six CSP gain and PT parameter combinations which should lead to the signal without undershoot or overshoot, with as high amplitude

as possible and the shortest rising time. Among these, the most preferred TC configurations defined are listed below:

- Setting 1 : Gain = 1mV/fC, Peaking-time = 15ns, TCC1 = 13.5pF, TCR1 = 19kΩ, TCC2 = 1.5pF, TCR2 = 23kΩ
- Setting 2 : Gain = 1mV/fC, Peaking-time = 20ns, TCC1 = 10.5pF, TCR1 = 27kΩ, TCC2 = 0.9pF, TCR2 = 20kΩ
- Setting 3 : Gain = 1mV/fC, Peaking-time = 35ns, TCC1 = 6pF, TCR1 = 31kΩ, TCC2 = 1.65pF, TCR2 = 23kΩ

Modifications in any of the PASTTREC configurations will result in variations in the detector performance. These configurations must be tested in a working detector under realistic conditions, and the configuration providing the best detection efficiency, energy resolution, and position resolution must be recognised. Evaluation of these configurations for detector operations is described in detail in Chapter 4.

Chapter 4

Tests of the detector and read-out

An FT detector prototype was built and was tested under a proton beam of momenta 3 GeV/c at the COSY, Forschungszentrum Jülich accelerator facility in early 2019. The measurement aimed to test the detector, read-out and data acquisition system under realistic conditions and benchmark the system's performance compared to the HADES-$\overline{\text{P}}$ANDA requirements in all the areas. The test setup, measurement goals, data analysis and results are discussed in this chapter. The findings of these tests provided important results for the final commissioning of the FT detector in the HADES experiment, performed in 2022, and the development of a track reconstruction analysis framework and the tests of the $\overline{\text{P}}$ANDA FT prototype. The findings have also provided important input to the technical design report for $\overline{\text{P}}$ANDA-DAQ. The results describing the detector performance are presented in the following sections.

4.1 Test setup

The FT detector prototype built for the tests had a modular structure with each straw module comprising 32 straw tubes arranged in two staggered layers (a double-layer). This double-layer of straw tubes is created by placing modules next to one another and mounting them to the same support frame. The FT prototype was built to resemble the $\overline{\text{P}}$ANDA FT5/FT6 stations with eight double-layers of straws of length 125 cm, each having 32 straws, shown in Figure 4.1. The layers were arranged in 0°, 5°, -5°, 0°, 0°, 5°, -5°, 0° inclination to the vertical axis respectively.

A scintillation detector (1) was placed before the FT prototype to provide the start time required to calculate the drift-time for the particles passing through the FT straws. A prototype of an Electromagnetic Calorimeter (EMC), a subsystem in the $\overline{\text{P}}$ANDA experiment, was used for the energy measurement. The detector systems' placement in the test beam area is shown in Figure 4.2. The straws, scintillator1 and the EMC shared a common data acquisition system, operating at a continuous data-taking mode with a free running clock of 20 kHz.

4.2 Measurement Goals

The measurements were made at the COSY accelerator facility at Forschungszentrum Jülich with a proton beam of momenta 3 GeV/c at an average intensity of 20

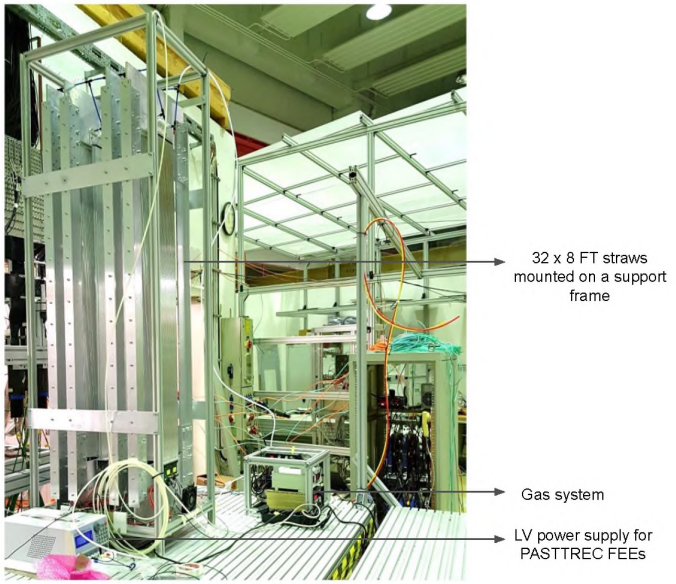


Figure 4.1: Layers of straw tubes mounted to the support frame and connected with the gas supply unit and the front-end electronic boards.

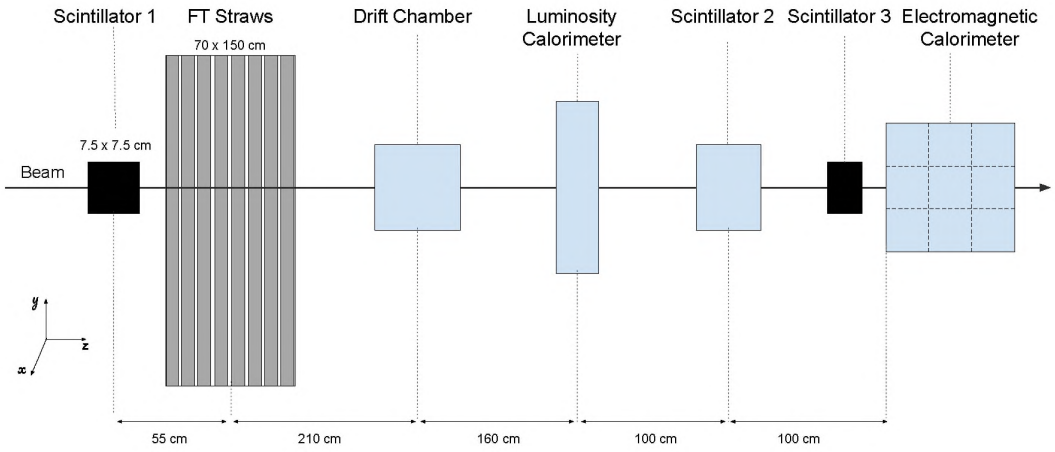


Figure 4.2: The schematic representation of the detector modules' placement during the proton beam tests.

kHz. The beam had a micro-spill structure with spills separated by 655 ns. One of the objectives of the in-beam measurements was to test the complete FT system, i.e. detector, read-out and data acquisition beam conditions. In this aspect, the goals for test beam measurements were as follows:

1. Detector and Read-out
   - Study the performance of PASTTREC configurations and detector efficiency at various HV settings.
   - Test the prototype gas system developed for HADES-$\overline{\text{P}}$ANDA FT.
2. Data acquisition
   - Continuous read-out using TRBv3 boards.

- Test the common $\overline{\text{P}}$ANDA DAQ with SODANet for multiple detector systems, i.e., FT straws, scintillator detectors and EMC.
- Tests of the data processing pipelines for $\overline{\text{P}}$ANDA DAQ.

The first goal was to confirm stable detector operation at high rates and its tracking resolution. In the test different configurations of the PASTTREC chip and HV settings of straws were examined to find the lowest HV setting and the discrimination level against the noise which provides high detection efficiency ($> 97\%$ per layer) at a low noise rate (< 100 Hz). Two configurations, based on discrimination thresholds 6 and 20 mV, were selected from the already performed tests with radioactive sources. They mainly differ in the rising time of the signal and the TC parameters as described in Table 4.1. The combination of the rise time, discriminator threshold level and HV setting are decisive factors for the position resolution and low ageing of the detector (ageing of straw tubes is described in Section 4.3.11). A compromise has to be found between the lowest possible HV (better for detector ageing) and the best signal-to-noise ratio and threshold settings. For the second goal, the in-beam test allows for a critical evaluation of the DAQ system performance under high-rate conditions. In particular, it is essential for the Event Building Network to determine its throughput and bottlenecks.

Furthermore, an algorithm for online track reconstruction, developed by the author of this thesis, was implemented in hardware and tested. Such an algorithm needs to be developed for PANDA FT online processing and implemented in an intermediate data processing stage between Data Concentrators and the EB network. Results of this test are described in Chapter 5.

Table 4.1: A table of configurations for the FT detector prototype used in test beam measurements. Data were collected for various detector HV, PASTTREC discriminator threshold and PASTTREC TC settings (1-3). These settings were described in Section 3.4.4.

		Detector High Voltage				
Discriminator Thresholds	TC Settings	1650 V 6 mV setting1	1700 V 6 mV setting1	1750 V 6 mV setting1	1800 V 6 mV setting1	1850 V 6 mV setting1
		1650 V 6 mV setting2	1700 V 6 mV setting2	1750 V 6 mV setting2	1800 V 6 mV setting2	1850V 6 mV setting2
		1650 V 6 mV setting3	1700 V 6 mV setting3	1750 V 6 mV setting3	1800 V 6 mV setting3	1850V 6 mV setting3
	TC Settings	1650 V 20 mV setting1	1700 V 20 mV setting1	1750 V 20 mV setting1	1800 V 20 mV setting1	1850 V 20 mV setting1
		1650 V 20 mV setting2	1700 V 20 mV setting2	1750 V 20 mV setting2	1800 V 20 mV setting2	1850V 20 mV setting2
		1650V 20 mV setting3	1700V 20 mV setting3	1750V 20 mV setting3	1800V 20 mV setting3	1850V 20 mV setting3

4.3 Data Analysis

The data collected from the in-beam tests have been analysed using dedicated offline software. Position resolution, energy resolution, detection efficiency and electronic noise for various configurations were the main features to be extracted from the data. The data were processed in several analysis stages that are further described in detail.

4.3.1 Analysis Software

The detector read-out system produces binary data output. The data analysis software has to be designed to extract information on the properties of the detector and the information essential to the physics goals of the experiment. This is detector efficiency, the spatial resolution of the reconstructed track and dE/dx in the case of $\overline{\text{P}}$ANDA FT.

The offline analysis software was developed to reconstruct particle tracks and analyse the data from the $\overline{\text{P}}$ANDA detector systems. It is based on the ROOT framework [26] and is written in C++. The offline software in its current form can analyse data from three detector systems, i.e., straw tubes (FT), EMC and a scintillator. It can be further extended to include other detector systems in the future. The most important classes in the software are described in Figure 4.3.

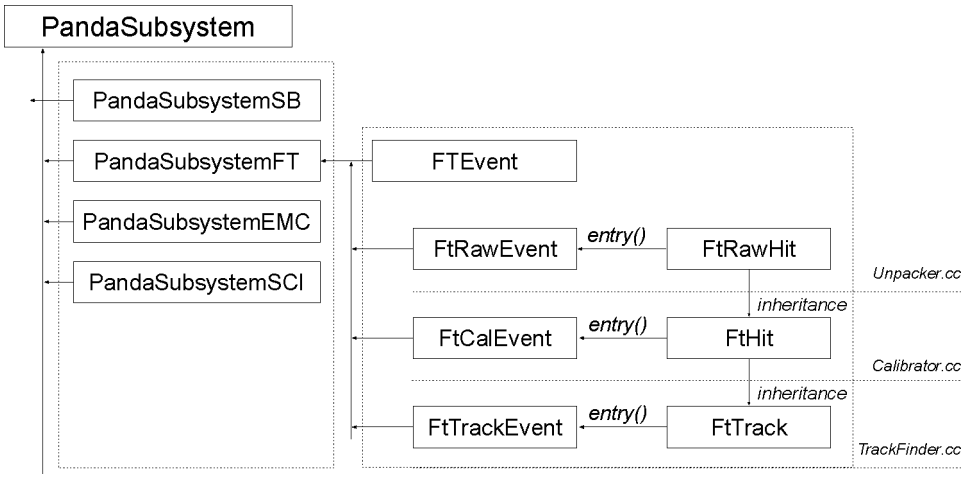


Figure 4.3: Schematic representation of the class design developed of the offline analysis.

- PandaSubsystems - Represents a detector subsystem or a super-burst in $\overline{\text{P}}$ANDA.
  - SB - Superburst carries information common to all the detectors like SB number and header words.
  - FT - Carries all the information from the FT detector.
  - EMC - Carries all the information from the EMC detector.
  - SCI - Carries all the information from the scintillation detector.
- Events - Carries all detector hits, tracks or clusters belonging to a time frame.

  - FtRawEvent - Carries 'FTRawHit' objects belonging to the event.
  - FtCalEvent - Carries 'FtHit' objects belonging to the event.
  - FtTrackEvent - Carries 'FtTrack' objects belonging to the event.

- Hits - Representing the most fundamental object belonging to an event in any analysis stage.
  - FtRawHit - Carries TDC channel and time information of a particle passing through a straw in the detector.
  - FtHit - Inherited from FtRawHit and carries calibrated time and geometry information of the straw hits.
  - FtTrack - A collection of FtHit objects belonging to a track along with the track parameters.

The data is processed in a pipelined structure. Every analysis stage takes an input file and produces an output file for the next stage. The software tools for those analysis stages are listed below.

- pdaq_unpacker - This is a binary data processing tool dedicated to decoding information from HLD files and saving it to the ROOT type files in the form of tuples. A 'PandaSubsystems' class is created for each detector system in the data.
- pdaq_ftcalibrator - Calibrates the TDC time and maps the geometry parameters to the straw data.
- pdaq_trackfinder - Performs event selection, track candidate selection and reconstructs low-resolution FT tracks.
- pdaq_ftdriftcal - Performs drift-time calibration and provides a time to-radius calibration curve for straws.
- pdaq_ftresolution - Performs high-resolution track reconstruction on straw data.

The inputs, outputs and the structure of output extracted information by the software tool are presented in Table 4.2. The software can be downloaded from the url: PDAQ_Tracking.

4.3.2 Data format

In the following text, the time duration between two triggers is called a time window. The data were collected at a clock rate of 20kHz corresponding to the time-window = 50 μs. The data in the given time window were read out by all the TRBv3s, packaged and stored in the PC by the event-building software. The data were stored in a binary form called HLD (HADES List Data), a standard inherited from the HADES experiment. In HLD each event has a header, followed by an arbitrary number of sub-events. The sub-events contain a header and a data block consisting of sub-sub-events and data blocks from individual FPGAs. The event header and sub-event headers are described in Figure 4.4 and Figure 4.5 [17].

Table 4.2: Stages of the offline data analysis software. The table shows input files for the macros which run the analysis, the processing macro, the output of the processing macro and the structure of the extracted information.

Input File name	Processing macro	Output file name	Output file structure
file_.hld	pdaq_unpacker	file_raw.root	FtRawHit, EMCRawHit, ScintRawHit
file_raw.root	pdaq_ftcalibarator	file_cal.root	FtHit
file_cal.root	pdaq_trackfinder	file_track.root	FtTrack
file_track.root	pdaq_ftdriftcal	file_dt.root	FtTrack
file_dt.root	pdaq_ftresolution	file_res.root	User histograms

The 32-bit wide data blocks in the HLD file collected during the test beam were generated by the TDCs in the read-out for the straw and the scintillator systems. The TDC data words are constructed from the TDC header, Epoch counter, Time word and TDC trailer. The TDC data words in the HLD file from the test experiment suffered from some artefacts like repeated time words (rising or trailing-time), missing leading or trailing time or some unrealistic difference between the leading and trailing-time. These artefacts were unique to the TDC version used in this test beam test and are resolved in future TDC versions. Either way, they must be eliminated in the first step, and the analysis software took care of it.

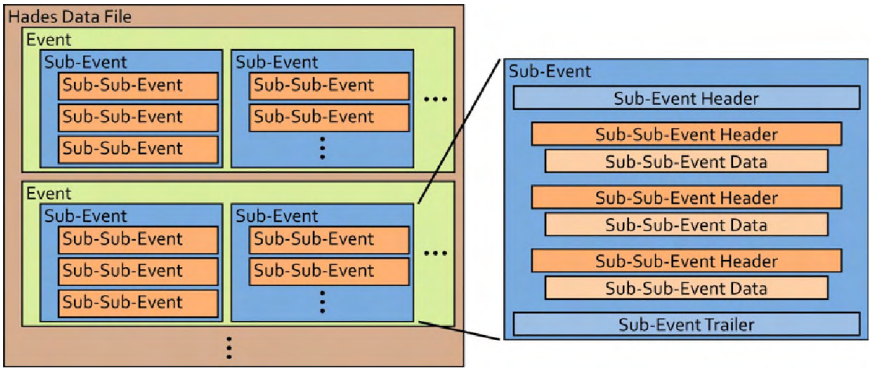


Figure 4.4: The structure of the hld file [20].

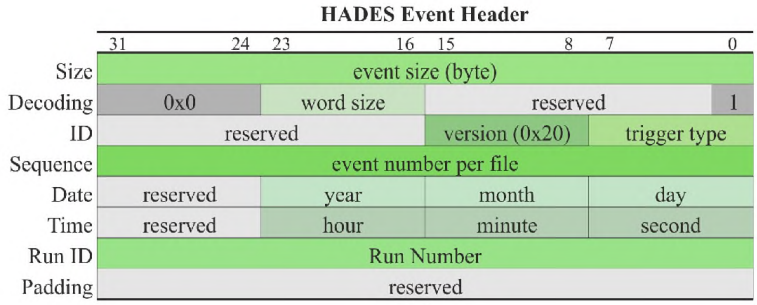


Figure 4.5: The structure of the event header. Followed by sub-events.

The first part of data processing was data unpacking from HLD binary files. The main task of the 'Unpacker' stage was to decode the headers, channel numbers and associated TDC time words to generate a more readable and structured output. The

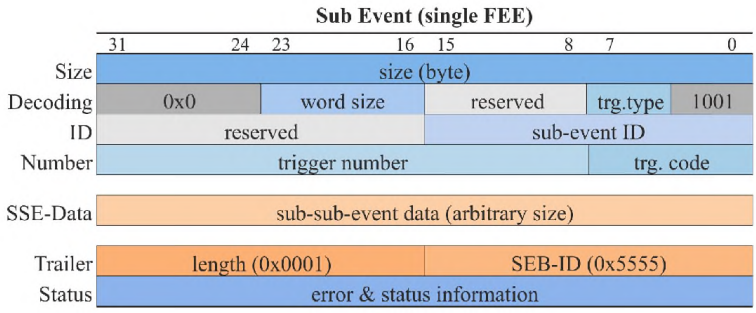


Figure 4.6: The schematic representation of the detector modules' placement during the proton beam tests.

TDC measures time as a sum of three types of counters. Fine time counter records time using Tapped Delay Line (TDL) method. An increment of this counter equals 10.6 ps. The coarse time counter has a period of 5 ns. The maximum time registered with this counter is 10.24 μs. The Epoch-counter measures time with a granularity of 10.24 μs. The maximum period that can be registered is around 45.8 minutes. These three counters are combined to reconstruct the signal generation time. An object called 'FtRawHit' representing a particle passing through the detector is created with: TDC ID, TDC channel number, TDC lead time, TDC trail time and the corresponding TOT.

```
FtRawHit :
TDC_ID          ID for the FPGA implemented with the TDC
TDC_channel     TDC channel number (0 to 48)
Lead_time       Time constructed for the rising edge of the signal
Trail_time      Time constructed for the falling edge of the signal
TOT             Difference between lead time and trial time
```

4.3.3 Geometry and Time calibrations

The data unpacked from the binary HLD to readable structure consists of only some basic information like TDC channel number and time representing a particle hit. In the next step of the analysis, the basic hit information from the unpacked data was translated into a hit inside the detector geometry. The detector geometry and the relation between the TDC channel and the detector geometry were predefined for the FT detector prototype in a lookup table. The parameters defining the detector geometry after the calibration are described in Table 4.3. This information will be further used to calculate a particle hit in the detector's x, y and z coordinates.

The time information (lead or trail time) for a hit is calculated with respect to a clock running on the TDC. This time calculated w.r.t this clock can be numerically different from TDC to TDC. For this reason, all the calculated lead times and trail time for the hits must be recalculated with respect to a common clock. For instance, the read-out used in the test beam at COSY used 2 TRBv3s with 4 TDCs. The offset in the clock between the TDCs in the same TRB as well as the TDCs in different TRBs is calculated and compensated for. This way, all detector hits from any part of the detector (connected to any TDC) are in a common timeline.

After the geometry and time calibrations, the 'FtRawHit' is updated as 'FtHit' with the following parameters :

Table 4.3: Parameters for detector geometry calibration.

Parameter	Description
Detector Geometry	
nStations	Number of FT stations
nLayers	Number of straw double-layers per station
nModules	Number of straw modules per layer
nStraws	Number of straws per module
nShortOffset	Position of short straw modules defined by the straw offset
nShortWidth	Number of straws in short straw modules
fStrawRadius	Straw radius in cm
fStrawPitch	Distance between two straws in cm
fLayerRotation	Orientation of layers in degrees
fTimeOffset	Offset for drift-time calibration
Lookup table for TDC channels	
TDC ID	TDC channel, Station, Layer, Straw, Cell (short or long straw)

```
FtHit :
Station      station number
Layer        double-layer in the station
Plane        plane in the double-layer (0 or 1)
Straw        straw number in the double-layer
Cell         straw type (0-short top, 1- short bottom, 3- long)
X, Y, Z        Coordinates of a hit in the detector
```

4.3.4 Event selection and hit filtration

The proton beam at COSY had a spill structure with spills separated by 655 ns, as shown in Figure 4.7. As it was mentioned above, the scintillator detectors (1) (see Figure 5.3) provided the reference time for drift-time calculation. The straws have a drift-time of 130 ns (at detector HV= 1800V and threshold= 10 mV, no magnetic field [14]). This value can extend depending on the statistical fluctuations in the ionization process, detector high-voltage, threshold and shaping configurations of the PASTTREC ASIC. In the case of FT prototype, the maximum drift-time was ~180 ns. It means that two hits can be well separated in one straw if their time difference is larger than 180 ns. Sometimes it is possible that hits within a spill can appear with a separation of less than the drift-time of the straw, resulting in a pileup of hits. Therefore the time difference between two consecutive scintillator hits was checked and those causing the pile-up hits were rejected (see Figure 4.7 marked in red). As the total number of pile-up hits amounts to less than 1% of the total hits, it was safe to extend the condition on the duration between two hits from 180 ns to 300 ns to increase the firmness of the filtration.

After rejecting the pileup hits within a time-window, these hits are further filtered to obtain clean track events. Although the pileup events were already eliminated, there can be more than one track in the $50\mu s$ time window. This is shown in Figure 4.8 displaying hit multiplicity in the reference detector (scintillator).

Straw hits belonging to individual tracks must be grouped from the pool of hits in the time window. All the straw hits within a time range of 0 to 500 ns with

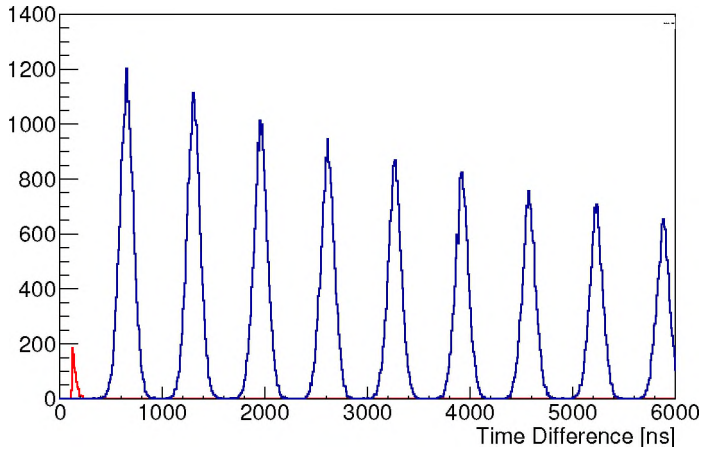


Figure 4.7: Spill structure of the proton beam represented by the time difference between the consecutive scintillator hits. Hits leading to the pileup of tracks in FT straws are recognized by the start detector with hits separated by less than 300 ns (red).

respect to the reference hit (hit in the scintillator) are grouped, and the outliers are rejected (much beyond the maximum drift-time). The FT detector prototype used for the tests has eight double-layers of straws as described in Section 4.1. A particle passing through the prototype must ideally register hits in all eight double layers (16 planes) to form a complete track. To obtain clean tracks, events with hits in all 16 straw planes are selected. The multiplicity of the planes before this selection is shown in Figure 4.8.

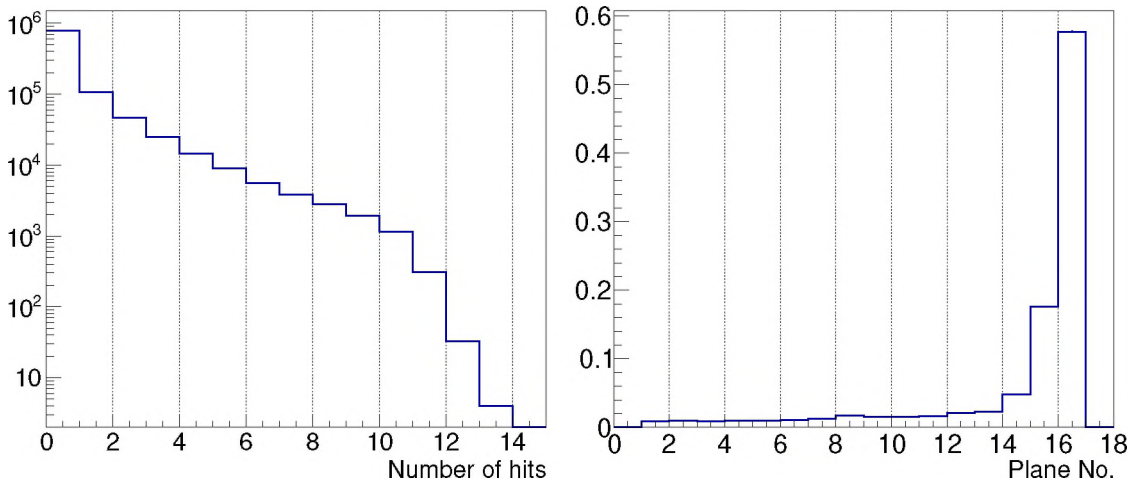


Figure 4.8: Left: Multiplicity of hits in the reference detector placed before the straws in a time window of 50 μs indicating the potential number of tracks in the straws. Right: Normalised multiplicity of detector planes before hit selection for track reconstruction. Only events with a multiplicity greater than 15 are later selected.

4.3.5 Track reconstruction

In this stage, the events selected from the previous stage of the analysis are further filtered to find the combination of hits to reconstruct the track's position from the coordinates of straw centres. This kind of tracking without utilising the drift-time information is called 'low-resolution' track reconstruction. As we are aiming at selecting only the clean track events and every detector double-layer has two planes of straws, every hit in a detector is expected to have a corresponding pair in the same double-layer. For this reason, only such 'hit-pairs' from each double-layer is selected. A combination of such hit-pairs (called clusters) from all the straw layers forms track candidates, as shown in Figure 4.9. An equation of track is constructed for every such cluster combination using a linear fit on the straw coordinates (x,z coordinates of the straw centres), and the cluster with the smallest sum of the squares (χ^2) is selected. Since only the vertical double-layers (0°) are sufficient to reconstruct tracks in 2D space, the inclined layers (±5°) are not used in the tracking. The residual of the track in this low-resolution track reconstruction is defined as the difference between the real track position and the straw centre along the x-coordinate. These residuals should be within the limit of the straw radius (0.505 mm). The track residuals calculated at this analysis stage are shown in Figure 4.10 and indeed show distribution spanned in this range.

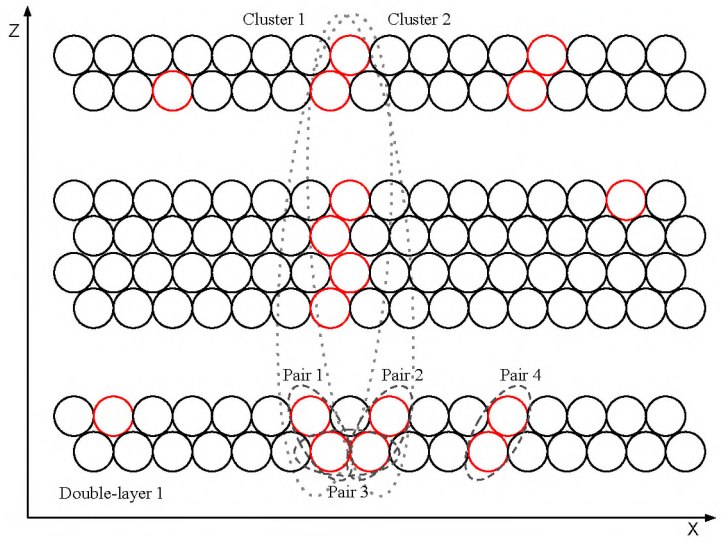


Figure 4.9: A schematic representation of the selection of track candidates in the x,z plane from clusters found in 4 double layers. Only vertical (0^0 layers are displayed.Beam axis is perpendicular to the (x,z) plane

In this stage, an object called 'FtTrack' is constructed from the hits belonging to the selected clusters. The parameters of the object are listed below.

```
FtTrack :
Size        Number of hits (FtHit) in the track.
Px0         Slope of the track in the x-coordinate
Px1         Track offset in the x-coordinate
ChiX        Chi-squared of the track fit
Ref.Time    Reference time for the track provided by the scintillator
```

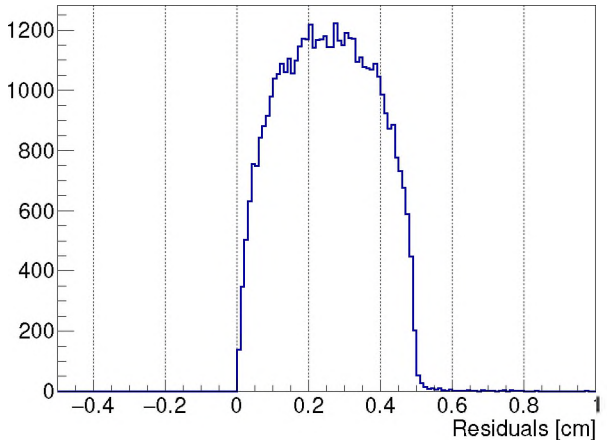


Figure 4.10: Track residuals calculated for the reconstructed low-resolution tracks.

4.3.6 Correlation of Space-to-Drift Time

The time taken by the ionised electrons to reach the anode is called drift-time. The drift-time is the most vital information required to reconstruct the position of the particle passing through the straw tube. The drift-time must be calculated and translated to coordinates in space for all the hits belonging to a track in this analysis stage. This correlation has to be established and calibrated for each straw tube. The methods used for drift-time calculation and calibration methods are described below.

Drift Time and drift radius

The scintillation detector placed before the FT straws provide the start time 'T0' that can be used to calculate the drift-time. The difference between the T0 and the lead time of a straw hit gives the drift-time 'dt_i'. The shortest distance between the anode and the particle track inside the straw is called the drift radius 'r_i' as shown in Figure 4.11. The straws have a radius 'r_{max} = 0.505 cm corresponding to a maximum drift-time 'dt_{max}' ≈180 ns (for FT prototype).

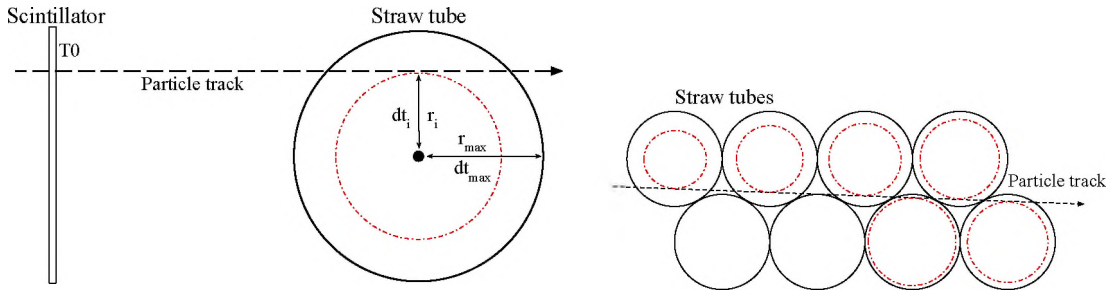


Figure 4.11: Left: Schematic representation of drift-time measurement with a scintillation detector and straws in the test beam. Right: Drift radius constructed for particles passing through a group of straws.

Time offset correction

Each straw tube in the detector operates like an individual detector. Measured drift-time distribution starts from a time offset that needs to be aligned for all straws.

The time offset for individual straws was calculated at 1/10th of the drift-time spectra and later corrected to a common value. The drift-time before and after offset correction is shown in the example of four straws in Figure 4.12.

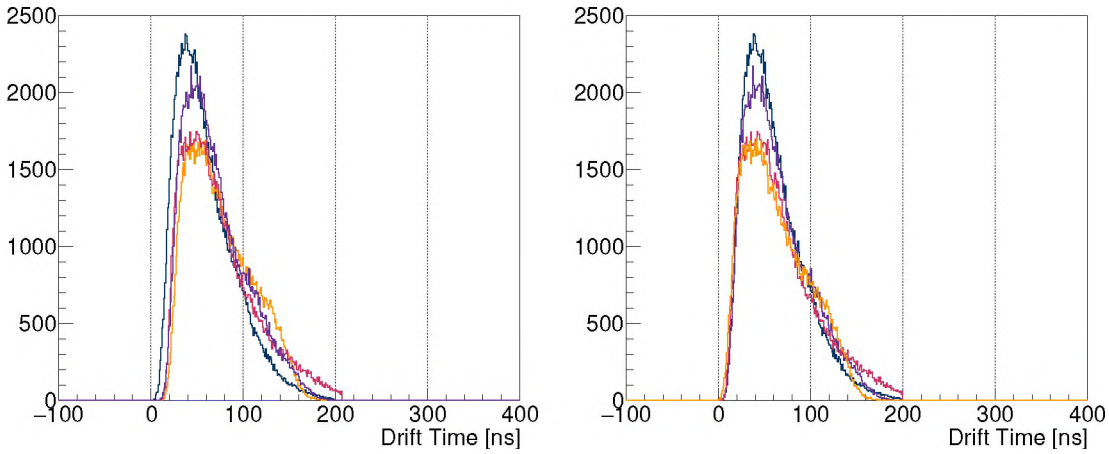


Figure 4.12: Left: Drift-time spectrum obtained from four straw channels. Right: Drift-time spectrum after time offset correction.

Uniform irradiation method

The relationship between the drift-time and the drift radius is not constant but varies with the electric field. A coarse relationship between drift-time and drift radius can be easily obtained after assuming the number of particle tracks passing through a given width of straw is uniform. Under this assumption, the drift radius *r(t)* is given by Eq. 4.1.

$$r(t) = \frac{R_{tube}}{N_{tot}} \int_0^{t_{max}} \frac{\mathrm{d}N_t}{\mathrm{d}t} dt' \tag{4.1}$$

Taking into account the finite TDC resolution (bin size) and the wire radius, Eq. 4.1 can be written as:

$$r(t) = \frac{\Sigma_{t=1}^{t_{max}} N}{N_{tot}} \cdot (R_{tube} - R_{wire}) + R_{wire} \tag{4.2}$$

Where, t is the drift-time bin index, N_{tot} is the sum of all the bin entries N (total number of hits), R_{tube} the radius of the straw and R_{wire} is the radius of anode wire in the straw. This equation assumes homogeneous irradiation and a constant detection efficiency along the straw radius. Spectra obtained from the FT straws under the test beam have a drift-time range of 0 to 180 ns. The spectrum is divided into 180 bins of width 1 ns each, and the correlation between drift-time and drift radius is obtained using this method described by Eq. 4.2 and shown in Figure 4.13. Such a correlation curve was produced for each straw double-layer (each double-layer has 1 module, i.e, 32 straws).

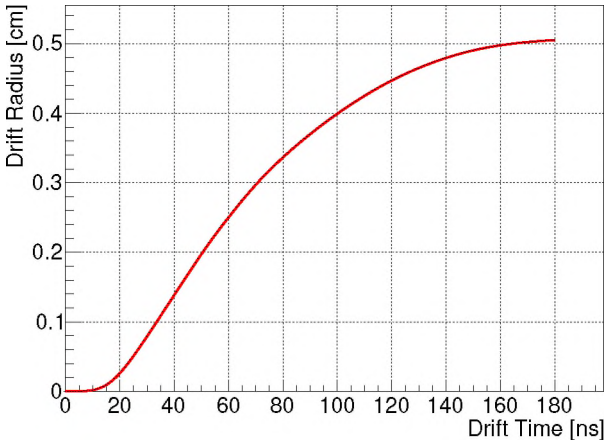


Figure 4.13: Drift radius as a function of drift-time determined using Eq. 4.2.

Iterative calibration method

The space-to-drift time correlation curve obtained from the uniform irradiation method is used to perform track reconstruction. The space coordinates of track hits in the straws are calculated, and the parameters of the track equation are determined. The shortest distance between the calculated drift radius *r(t)* and the reconstructed track r_f is the residual and is given by Eq. 4.3.

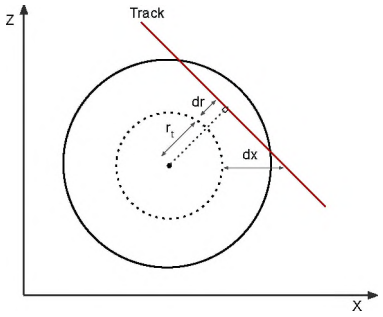


Figure 4.14: Drift radius as a function of drift-time determined using equation.

$$dr = r(t) - r_f \tag{4.3}$$

The drift-time radius calibration could be improved by an iterative procedure using

$$r^{i+1}(t) = r^i(t) - dr \tag{4.4}$$

The mean residual *dr* is the correction offset value calculated for each time bin as shown in Eq. 4.3 and Eq. 4.4. The space-drift-time calibration curve is corrected with the offsets obtained for each time bin. This procedure is repeated until the mean offset in the straw double-layer for *dr* for all the time bins is minimised as shown in Figure 4.15. This iterative method accounts for the correlations between different hits on a track and between different tracks [27]. This way, iterations can converge the correction offset value to zero with a small number of tracks and improve space-to-drift time correlation precision.

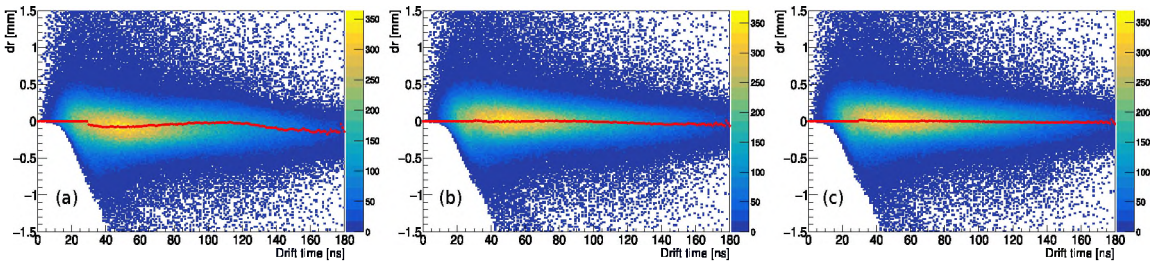


Figure 4.15: An example of residuals as a function of drift-time for one straw double-layer after three iterations (left to right). The red line indicates the converging mean residual value after iterative calibration.

The coordination obtained from the corrected space-drift-time correlation curves is used to reconstruct high-resolution tracks. The residuals calculated for these tracks are presented in Figure 4.16.

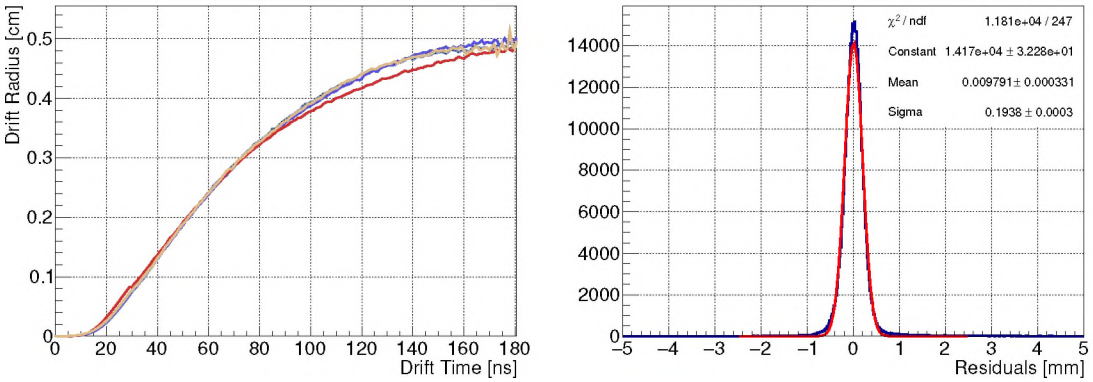


Figure 4.16: Left: Drift radius as a function of drift-time calculated after space-drift-time calibrations. Four coloured curves represent the correlations for the four straw double-layers in the detector. Right: Residuals calculated for the reconstructed high-resolution tracks in the entire detector operating at 1700 V.

4.3.7 Spatial resolution

The high-resolution tracks were reconstructed using the χ^2 fit on the obtained space coordinates as shown in Eq. 4.5.

$$\chi^2 = \sum_{t=1}^{N} \frac{(r_t - r_f)}{N\sigma_a^2} \tag{4.5}$$

Where r_t is the measured space coordinate and r_f is the coordinate obtained from the track fit, σ_a is the average spatial resolution of the straws, and N the number degrees of freedom (6 in this case, as tracking included 4 double-layers of straws, i.e 8 straws with 2 used as constraints). The χ^2 distribution of the track was calculated for average spatial resolution σ_a ranging from 150 μm to 300 μm in steps of 10 μm. The distribution that compares closest to the theoretical χ^2 contains $\sigma_a = 190\mu$m [28]. This is comparable to the expected resolution (200 ns [10]) and is shown in Figure 4.17.

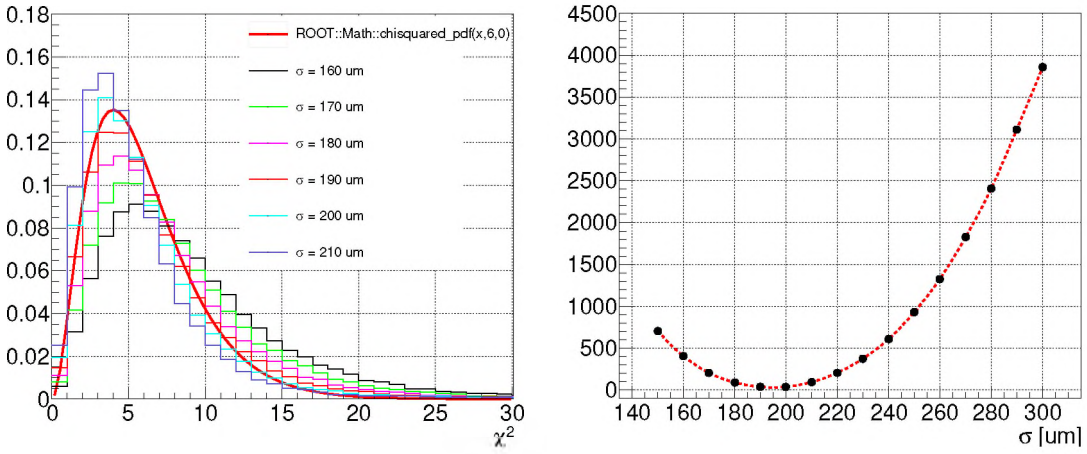


Figure 4.17: Left: The χ^2 distribution of the reconstructed tracks calculated for various average spatial resolution σ_a values fitted with theoretical χ^2 distribution with N=6 d.o.f (Red). Right: Sum of the squares calculated by comparing theoretical χ^2 distribution to the various χ^2 distribution of the reconstructed tracks indicating best fit at $\sigma_a = \sim 190$ μm.

4.3.8 TOT calibration

The TOT is proportional to the amplitude of the signal produced in the straw due to the charge ionised by the energy loss of the passing particle. The energy loss across the straw is not constant and depends on the particle path length in the straw. Data collected during test beam time allowed us to observe TOT dependence on track path length given by drift radius. The TOT offset with respect to the mean TOT is calculated for each time bin (1 ns) and corrected by a factor 'F' given by Eq. 4.6.

$$F^i_{crr} = \frac{TOT_{mean}}{TOT_i} \tag{4.6}$$

Where TOT_{mean} is the mean TOT of the particle in the detector and TOT_i is the TOT corresponding to the drift-time of i ns in a straw module. The correlation between TOT and drift-time before and after the calibration is presented in Figure 4.18.

Furthermore, the ionization for a given path length can fluctuate statistically according to Landau distribution [29]. Occasionally, a particle with the same momentum will leave more ionization clusters and sometimes less. This can lead to higher or lower TOT values. When tracks are constructed from many layers of straws, a so-called truncated mean can be performed to eliminate such TOT values and significantly improve the resolution. In this operation 20% of the highest and lowest TOT values are eliminated and the mean TOT is calculated from all the straws in a track. Such truncated mean TOT calculated for tracks passing through four double-layers of straws is presented for the prototype detector operating under two different high-voltages in Figure 4.19.

In the $\overline{\text{P}}$ANDA experiment, TOT measurement straw layers will be used to identify proton/pion/kaons in the momentum range $p < 1$ GeV/c. Particles of the given momenta can be identified and resolved according to the Bethe-Bloch low relating ionisation loss dE/dx with $\beta\gamma$. The energy loss reconstructed from the

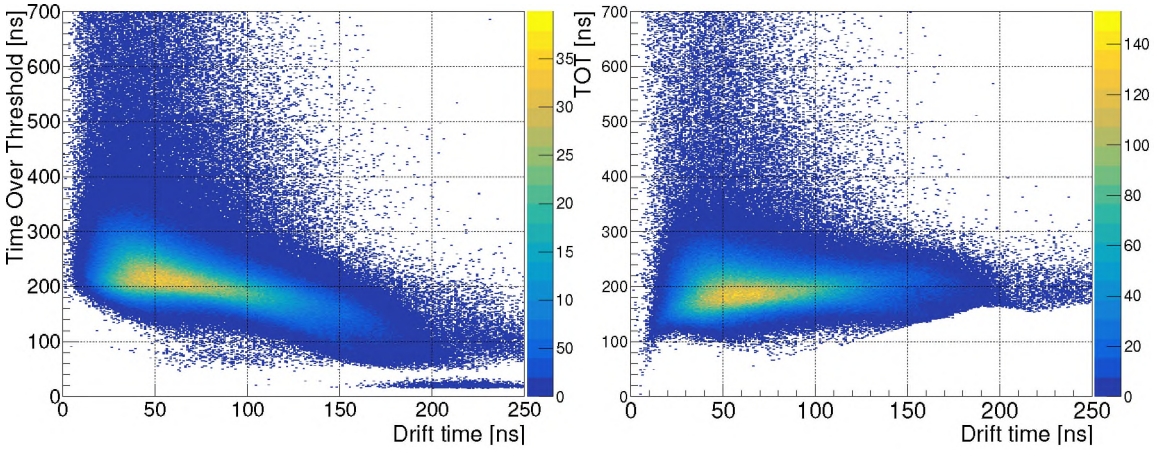


Figure 4.18: Left: TOT as a function of drift-time before calibration. Right: TOT as a function of drift-time after calibration.

simulations studies of different particles in $\overline{\text{P}}$ANDA straws is plotted for various momenta and shown in Figure 4.20 (left). The sample is composed of five types of charged particles (electrons, muons, pions, kaons and protons). The regions for different particles have been identified as bands, with a mean value and an amplitude (shown in black lines) [10]. The separation power of the TOT, as defined below, is used to evaluate the TOT resolution of the detector. The separation power is given by Eq.4.7.

$$sep = \frac{Mean_1 - Mean_2}{\sigma_1/2 + \sigma_2/2} \tag{4.7}$$

where, $Mean_1$, $Mean_2$ are the mean of the TOT spectra and σ_1, σ_2 are the sigma of the TOT spectra obtained for the two induced charges. The relation between the induced charge and TOT is described in Section 3.1.2.

In the case shown for the FT prototype straws in Figure 4.19, the TOT obtained from protons at two different detector high-voltage is virtually identical to the case where two different kinds of particles are inducing charges in the straw tubes at a given momentum. This can be confirmed by calculating the charge induced (using Eq. 3.4) at detector high-voltage 1700V and 1800V. The charge induced at detector high-voltage 1800V is 2.46 times the charge induced at 1700V and the separation power of mean TOT (obtained from Figure 4.19) is equal to 2.99 (SEP_{FT}). This is equivalent to the charge induced by protons and pions at 0.7 GeV/c as shown in Figure 4.20 (left, red dotted line, 5×2.46). The simulation studies performed using 27 double-layer straws (54 straws per track) indicate a separation power between 0.7 GeV/c protons and pions is equal to $\approx$8 (SEP_{ppi_sim}) as shown in Figure 4.20 (right, black dotted line). The standard deviation σ calculated for the truncated TOT is inversely proportional to $\sqrt{n}$, where n is the number of samples (i.e straws used to calculate the truncated mean TOT). As the mean TOT calculated from FT prototype tracks use only 8 straws compared to 54 straws used in the simulation studies, SEP_{HV_FT} must be scaled by a factor of 2.6 (i.e $1/\sqrt{54} \div 1/\sqrt{8}$). Thus, it is observed that the separation power for FT prototype straws is comparable (SEP_{HV_FT} = SEP_{ppi_sim} = $\approx$8) to the results obtained from PANDA simulation studies.

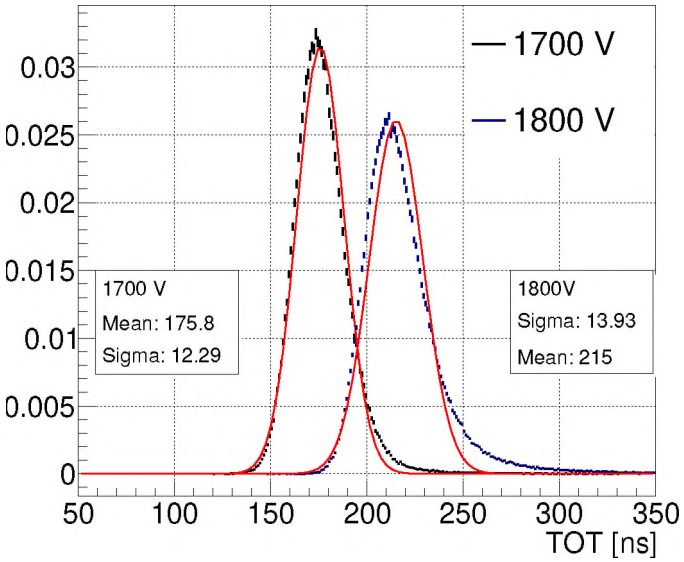


Figure 4.19: Truncated mean of TOT obtained from p= 3 GeV/c proton (MIP) tracks passing 8 straws for the detector operating at high-voltages 1700V and 1800V respectively. The spectra are fit with a Gaussian and the obtained mean and σ are used to calculate separation power.

4.3.9 Detection efficiency

The average detection efficiency of a single straw plane was determined by a fit of the plane multiplicity of reconstructed tracks shown in Figure 4.21.

The experimental distribution was determined as follows. Two hits in the first double layer and the last straw layer were requested for the track reconstruction. Tracks were fitted with a linear equation, as explained in previous sections, and a virtual corridor with a width of 5 straws along-track direction was constructed to search for fired planes. The measured number of straw planes (multiplicity) in this virtual corridor provides the measured probability distribution required for efficiency calculation. One should note, that any accidental coincidences affecting the efficiency calculations were rejected by selecting hits from those belonging to this 'virtual corridor'.

A function which was applied in the fit was the binomial distribution, described by Eq. 4.8.

$$P(X) = \frac{n!}{(n-X)!X!} \cdot (p)^X \cdot (q)^{n-X} \tag{4.8}$$

Where $P(X)$ is the probability of success, i.e.number of tracks with hits detected in X straw planes, n is the total number of straw planes which can contribute to the track (it equals to 12 planes, not 16 because 4 planes belonging to the first and the last layer required for track reconstruction as considered as constraints), p is the probability of success which is equivalent to the detection efficiency of a single plane and q is the probability of failure (equals to *1-p*).

The detection efficiency depends on many factors like the detector's high voltage, the configuration of the FEB, gas mixture, etc. Optimal detector settings were found for the Ar: CO2 gas mixture (proportioned at 90:10) with a high-voltage of 1750V,

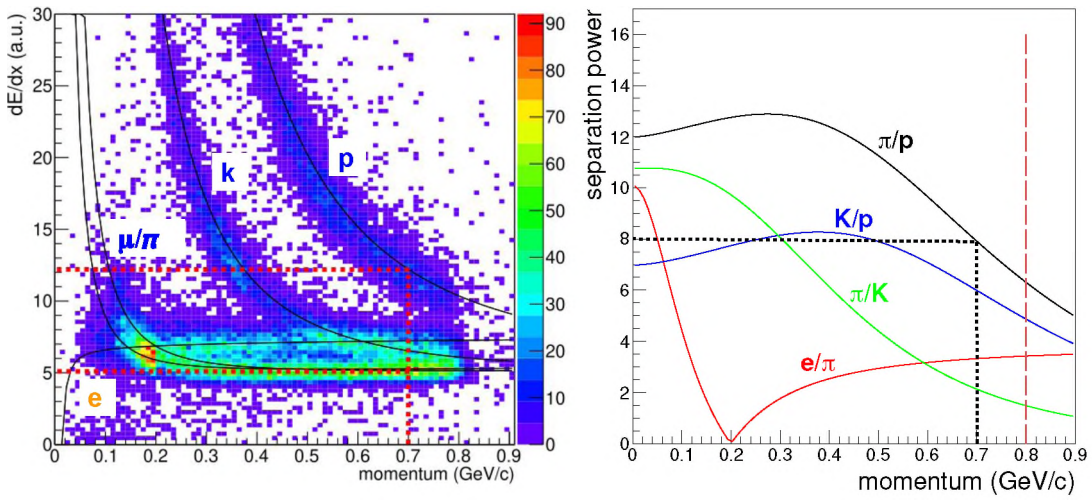


Figure 4.20: Left: Distribution of dE/dx truncated mean values vs reconstructed momentum for electrons, muons, pions, kaons and protons reconstructed from the simulation studies of PANDA STT. The superimposed lines (black) are the mean value of the band (the tracks have been fitted by the Kalman filter with the mass hypothesis of muon). Right: Separation power in the PANDA straws for the bands built with particles from simulated tracks. The vertical line at 0.8 GeV/c is the momentum threshold to perform the particle identification in the PANDA straws [10].

PASTTREC discriminator threshold of 6 mV, and signal peaking-time set to 20 ns (comparison with other configurations is discussed in Section 4.4). The measured probability of success was 0.8 (12 straw planes) as shown in Figure 4.21. This presents a high detection efficiency of $\approx$ 98% straw tubes, in compliance with the $\overline{\text{P}}$ANDA FT design requirements.

4.3.10 Effects of straw deformations

The straw tubes are cylindrical chambers with an anode wire stretched along the cylindrical axis. The over-pressured gas mixture makes the straws self-supporting. Deformation of the straws (Eg. bending) caused by mechanical factors or by physical damages will break symmetry in the straws and hence affect drift-time and the TOT distributions. The distance between the anode wire and the straw cylinder has to be congruent along the cylindrical axis as shown in Figure 4.22. In that case, the drift-time and TOT obtained from a charged particle traversing through either side of the straw are identical. The drift-time will be affected if the straws are deformed, and the anode wire is displaced to either side perpendicular to the beam axis (if $\Delta X1 \neq \Delta X2$). In such a case, if the straw is subjected to uniform irradiation, particles passing through one side of the straw will have a drift-time shorter compared to those passing on the other side. Another similar effect is caused when the anode wire position is distorted along the beam axis (if $\Delta Z1 \neq \Delta Z2$). In this case, the drift-time of particles passing through either side of the straw will be similar, but the TOT will be distorted. The amplitude of the signal induced by the drifting ionisation electrons will be smaller but longer in duration, leading to longer TOT values. These effects of straw deformation on drift-time and TOT have been studied

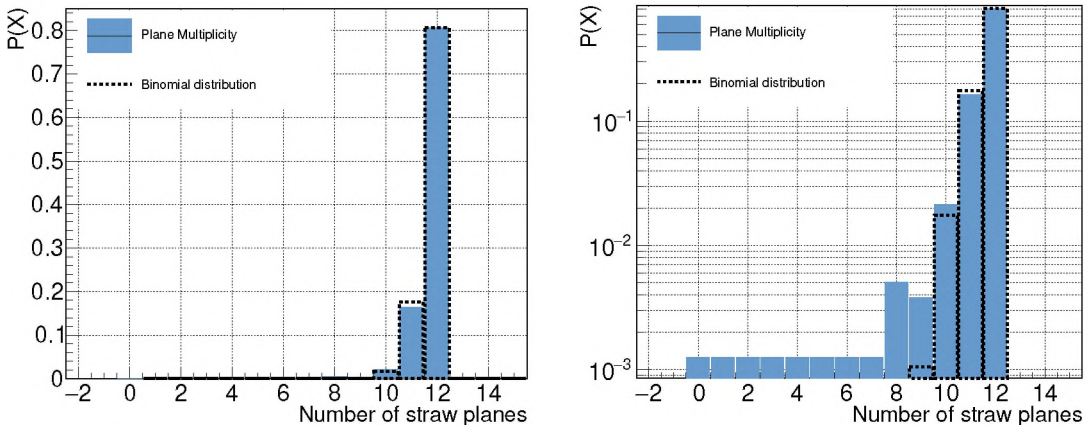


Figure 4.21: Left: Multiplicity of straw planes with track hits *P(X)* compared with the binomial distribution calculated assuming efficiency $p = 98\%$ (dashed black). Right: Multiplicity of straw planes with track hits *P(X)* compared with the binomial distribution in logarithmic scale.

for the FT detector prototype under the beam. Two out of eight straw modules (32 straws per module) in the FT prototype detector had deformations affecting the DT and TOT. The drift-time and TOT obtained from such straw modules have been presented in Figure 4.23. The effect of these deformations on the spatial resolution and the energy resolution of the straws have not been studied here and are the work for the future. However, observations of such deformations via the correlation of drift-time vs TOT provide a valuable quality measure for straws and will be carefully monitored in the production process.

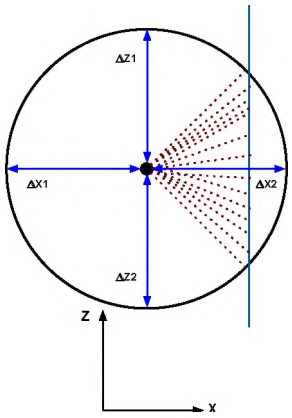


Figure 4.22: Schematic representation of signal generation due to a particle passing through the straw where the anode wire is in the exact centre.

4.3.11 Ageing of straw tubes

The gain degradation in the straw tubes due to prolonged irradiation is called the ageing effect. The contaminants in the straw materials or in the gas mixture can decompose under the charge density in the straw tubes and form polymeric deposits on the electrodes. This can cause a drop in the charge gain in the straw tubes. An-

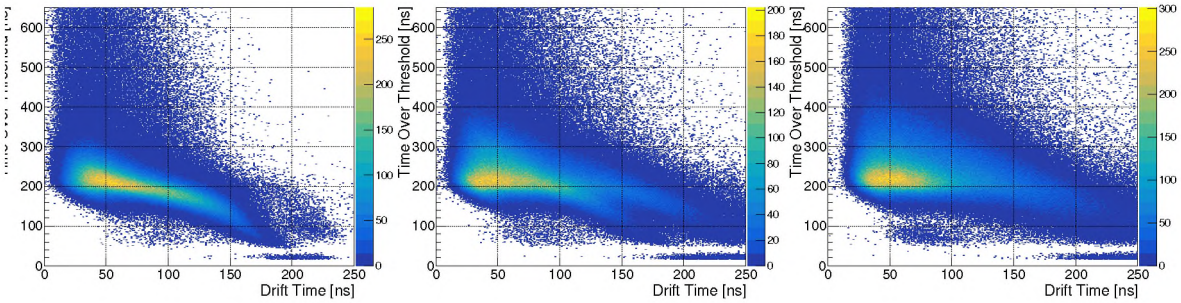


Figure 4.23: TOT as a function of DT for normal straw and deformed straw modules (32 straws each). Left: Normal straws with anode wire at the centre, i.e. $\Delta X1 = \Delta X2$ and $\Delta Z1 = \Delta Z2$. Centre: Deformed straws with the anode wire shifted to a side forming a "double-leg" structure, i.e. $\Delta X1 \neq \Delta X2$ and $\Delta Z1 = \Delta Z2$. Right: Deformed straws with the anode wire shifted forward causing a larger TOT spread, i.e. $\Delta X1 = \Delta X2$ and $\Delta Z1 \neq \Delta Z2$.

other cause of ageing is the oxidation of the gold-plated anode wire due to chemical reactions. The $\overline{\text{P}}$ANDA $p\overline{p}$ experiment at 15 GeV/c has will have interaction rate of $2{\times}10^7$. The particle flux experienced by the straw tubes close to the beam pipe is estimated to be 25 kHz cm $^{-2}$ [14]. The straw tubes have a gas gain of $5{\times}10^4$ at a detector high voltage of 1800V. The accumulated charges in 10 years of $\overline{\text{P}}$ANDA FT lifetime are estimated to be Q/I $\leq$ 0.75 C/cm for distances from beam axis x $\geq$ 40 cm. This reaches Q/I = 6 C/cm for smaller distances in FT1, as shown in Figure 4.24.

The tests performed with radioactive sources and FT prototypes have indicated a gain drop of 8% for an accumulated charge of 0.63 C/cm [30]. This ageing effect, if not reduced, would demand the replacement of the straw modules closer to the beam-line in FT1 and FT3 after a few years of $\overline{\text{P}}$ANDA operation.

The gas gain in the straw tubes is proportional to the voltage applied to the anode. Reducing the detector's high voltage from 1800 V to 1700 can reduce the gas gain from 5×10^4 to 2×10^4. This way, the charge load on the straws can be reduced, and the ageing effect can be significantly reduced. Therefore, the high efficiency of straws at HV=1750V demonstrated in the test with the FT prototype is very important in the context of ageing reduction. Furthermore, the steps taken to improve the signal-to-noise ratio in this work will allow us to reduce the discrimination threshold, further allowing us to decrease the detector's high-voltage. The detector and readout operational configurations are carefully selected with the above-described goal. These selections are discussed further.

4.4 Selection of the FT operational parameters

The data collected from the beam tests at COSY, tests with radioactive sources and noise studies described earlier are used to evaluate the detector's performance for various operational parameters. The performance of the system is evaluated based on spatial resolution, energy resolution, detection efficiency, electronic noise, and ageing-effect for the operational parameters listed below:

- Detector high-voltage

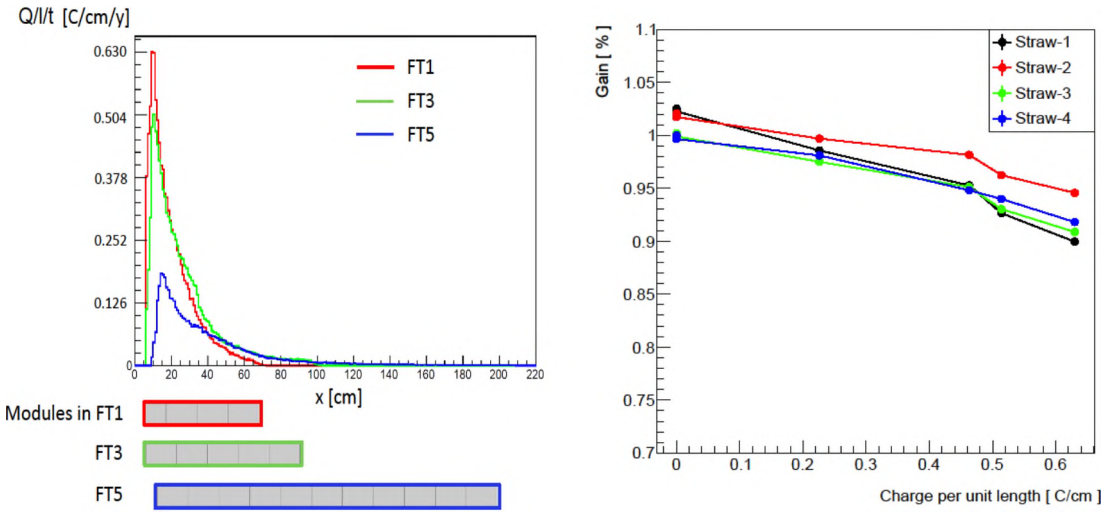


Figure 4.24: Left: The accumulated charge in C/cm/year expected in the $\overline{\text{P}}$ANDA high luminosity mode, at the highest beam momentum of 15 GeV/c, presented as a function of the x-coordinate (perpendicular to the beam direction at the target) in the horizontal symmetry plane (y = 0), for the tracking stations FT1, FT3 and FT5 [14]. Right: Gain drop in straws for an accumulated charge of 0.63 C/cm.

- Discriminator threshold
- peaking-time and tail-cancellation setting
- Amplification gain in the PASTTREC

Changing one of these parameters might improve the detector's performance in some aspects but worsen the overall performance of the detector. A set of parameters with balanced performance across all the criteria has to be selected.

Spatial resolution

The time precision of the measured signals determines the resolution of the reconstructed tracks. The "time-walk effect" caused by the change in signal amplitude at the given discriminator threshold can reduce the precision of time measurement. The precision in time measurement improves with the increase in the detector's high voltage as the time-walk in the signal decreases. The walk effect in time measurement can also be minimised by discriminating the detector signal at a lower amplitude. On the other hand, the electronic noise defines a lower limit for the threshold.

In order to find the optimal settings scan of HV and discrimination levels was performed. The drift-time spectra for detector high-voltage varying from 1650 V to 1850 V and for discriminator thresholds 6 mV and 20 mV are presented in Figure 4.25. Similarly, the walk effect can be minimised by decreasing the peaking-time in the PASTTREC configuration (setting 1-3). The drift-time spectra for the TC settings with different peaking-times are shown in Figure 4.26.

The spatial resolution was calculated for five different detector high-voltages, two different discriminator thresholds, and three TC settings using the method described in Section 4.3.7 and are shown in Figure 4.27. The results indicate that spatial

resolution improves with the increase of the signal amplitude (corresponding to increasing of the high-voltage) and a decrease of the peaking-time and threshold.

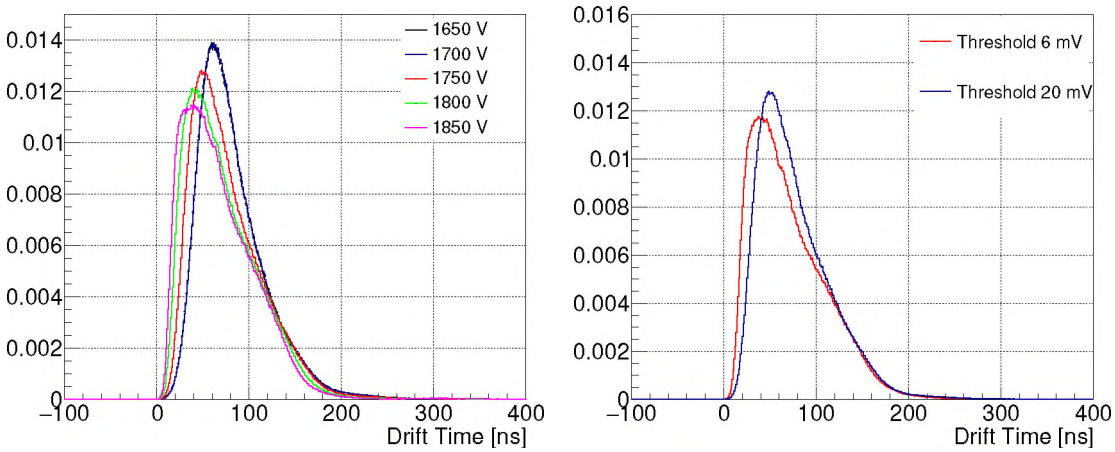


Figure 4.25: Left: The drift-time spectra for detector high-voltage varying from 1650 V to 1850 V, discriminator thresholds set 20 mV and peaking-time 20ns. Right: The drift-time spectra for varying discriminator thresholds, detector high-voltage 1750 V, and peaking-time 20ns. Improvement in time measurement is observed with increasing high-voltage and decreasing the threshold in the PASTTREC.

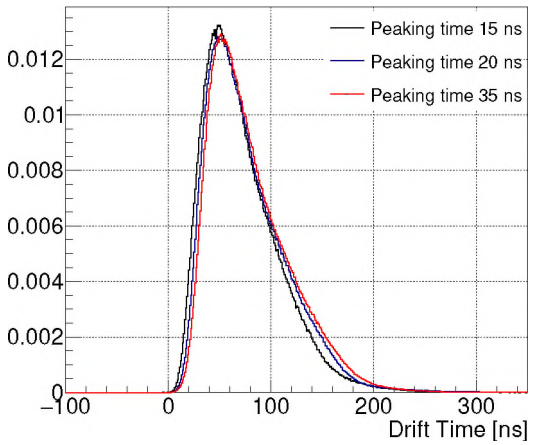


Figure 4.26: The drift-time spectra for varying peaking-time, detector high-voltage 1750 V, and threshold 20 mV. Improvement in time measurement can be observed by decreasing the peaking-time in the PASTTREC.

TOT resolution

The increase in TOT with the increase of the charge is clearly visible, however, as one can see it is not proportional. This is the feature of TOT vs charge characteristics, discussed in Section 3.1.2. A correlation between the induced charge, varied by the high-voltage increase (calculated by Eq. 3.3), and TOT measured in FT prototype is shown for p= 3 GeV/c protons (MIP) in Figure 4.28. The separation power of

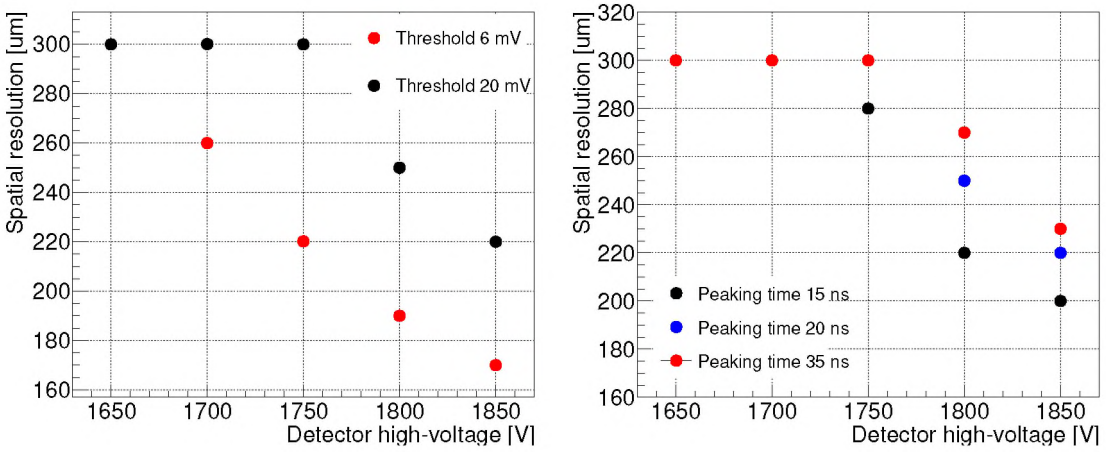


Figure 4.27: Left: The spatial resolution calculated for varying PASTTREC thresholds and varying detector high-voltage. Right: The spatial resolution is calculated for varying PASTTREC peaking-times and varying detector high-voltage. The spatial resolution improves with the increase in the detector high-voltage and decreases in the PASTTREC threshold, and decrease in the PASTTREC peaking-time.

the TOT, as defined in Section 4.3.8, is used to evaluate the TOT resolution of the detector for various PASTTREC settings.

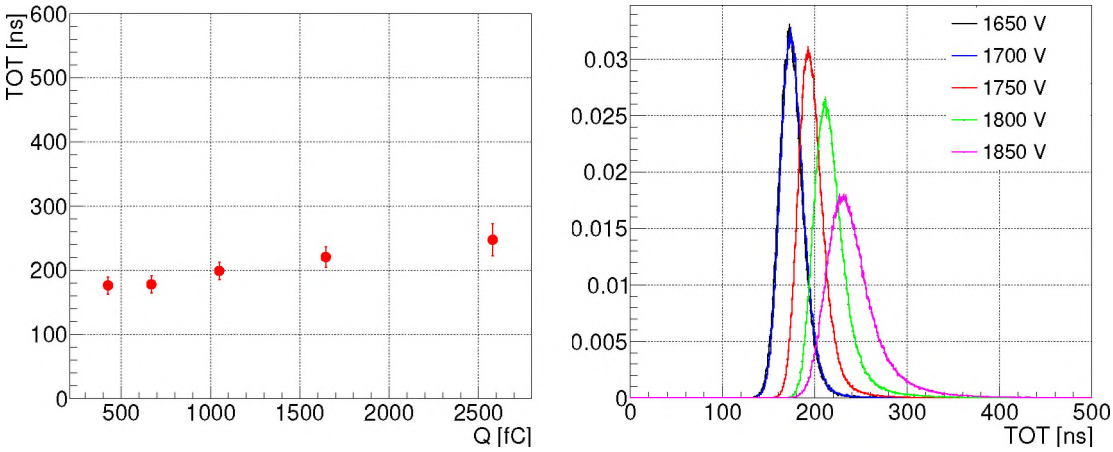


Figure 4.28: Left: TOT as a function of charge calculated by varying the detector high-voltage from 1650 V to 1850 V operating with PASTTREC threshold set to 20 mV. A linear correlation can be observed in the detector operational region. Right: TOT measured for varying the detector high-voltage and PASTTREC threshold set to 20 mV. An increase in the mean value and the standard deviation in the TOT increases with the increase in the detector's high voltage is observed.

The threshold position can strongly influence the separation power in the PASTTRECs. Too low a threshold deteriorates separation power but increases detector efficiency and separation resolution. Hence an optimum has to be found. Furthermore, electronic noise limits the lowest possible threshold position. It can be seen in the measured TOT for the data collected at a threshold set to 6 mV which shows an oscillating pattern, as shown in Figure 4.29. The separation power is compared for

the three TC settings (setting1, setting2, and setting3) with different peaking-times and the 20 mV threshold. The best separation is observed for setting3 with 35 ns peaking-time as shown in Figure 4.30.

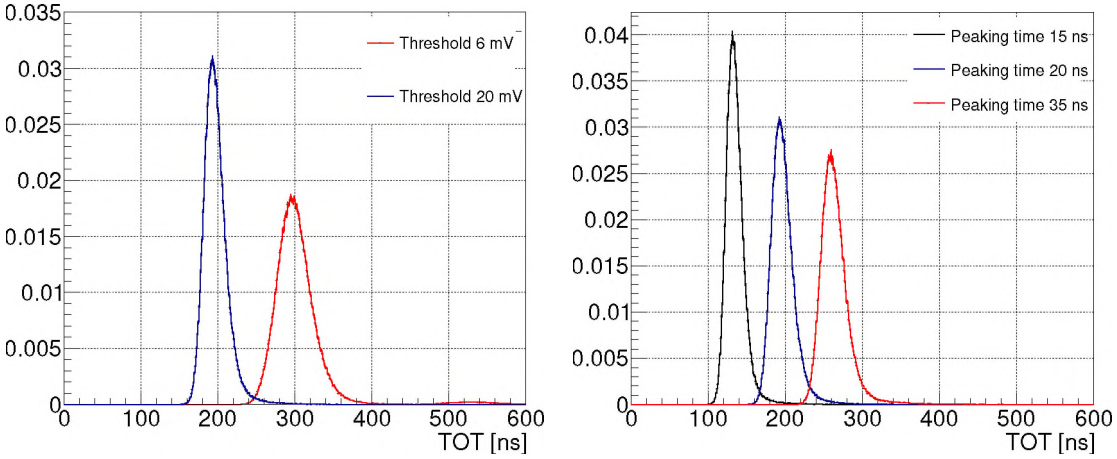


Figure 4.29: Left: The TOT measured for PASTTREC threshold set to 6 mV and 20 mV. TOT values are smearing at 6 mV due to the higher noise in the detector setup used in this measurement. Right: The TOT measured for PASTTREC peaking-time set to 15 ns, 20 ns and 35 ns.

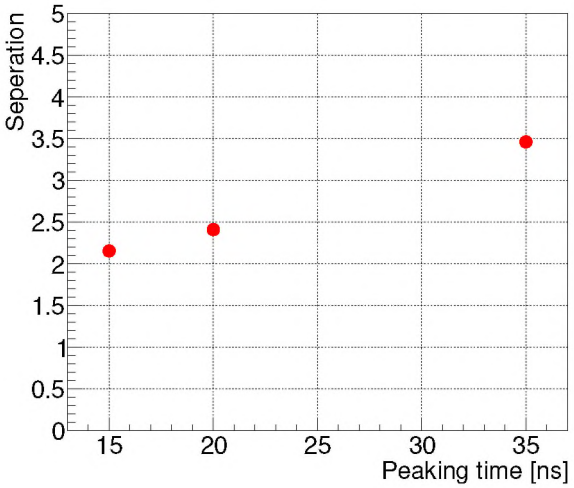


Figure 4.30: Separation power calculated for PASTTREC peaking-time set to 15 ns, 20 ns and 35 ns.

Detection Efficiency

The detection efficiency of the FT prototype was investigated as described in Section 4.3.9 for various thresholds and TC settings at different detector high voltages. The detection efficiency is sensitive to the threshold level. It is expected to be better at lower thresholds, as some low-amplitude signals might get discriminated against if the threshold is high. This difference in detection efficiency can be observed in

Figure 4.31 (left), especially at lower detector high-voltages. The efficiency increases as the signal amplitude increase at higher voltages. Changing the TC-setting can also lead to a change in the signal amplitude, further leading to varied detection efficiency. It is observed that setting3 with 35 ns peaking-time presents the best detection efficiency, but setting2 with 20 ns peaking-time has uniform efficiency for all the detector high-voltages. These results indicate that the detection efficiency improves by increasing the detector's high voltage, reducing the threshold in the PASTTREC and using the TC-setting with a longer peaking-time.

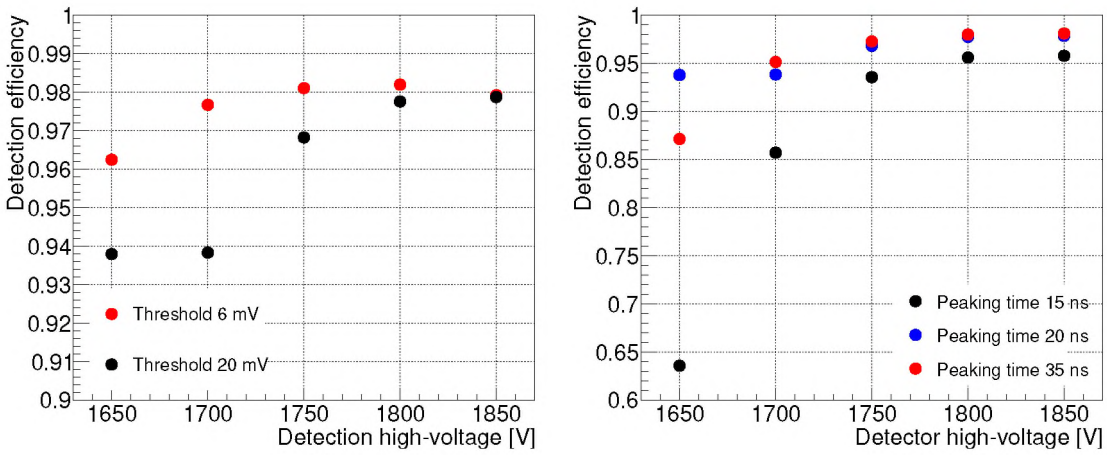


Figure 4.31: Left: Detection efficiency calculated for PASTTREC thresholds set to 6 mV and 20 mV and for varying detector high-voltage is set to 1750 V. Right: Detection efficiency calculated for PASTTREC for peaking-times 15 ns, 20 ns, 35 ns and for varying detector high-voltage. The detection efficiency is observed to be optimum at 1750 V.

Noise

The electronic noise calculated using the s-curve method indicates lower noise at higher peaking-times (20 ns and 35 ns) as shown in Figure 4.32 (left). The noise in the PASTTREC channels is also observed to be lowest for the highest amplification gain (4 mV/fC) as shown in Figure 4.32 (right). The average noise in the PASTTREC channels is a little over 1 mV. This is five sigmas below the standard operation threshold (20 mV). It is an important observation as it indicates the scope for reducing the threshold (which will also improve the time-space resolution) or decreasing the detector's high voltage (which will reduce the ageing effect).

Gain selection

Reducing the detector's high voltage will result in reduced gain and cause a reduction in the signal amplitude. This reduction in the signal amplitude can be compensated by increasing the gain in the PASTTREC. This is desired as the noise in the PASTTREC is lowest at a gain of 4 mV/fC. This change in gain and detector high voltage should not reduce the performance of the detector (spatial and energy resolution, detection efficiency etc.) but rather improve the performance. The FT detector prototype was irradiated with the ^{55}Fe radioactive source in laboratory conditions,

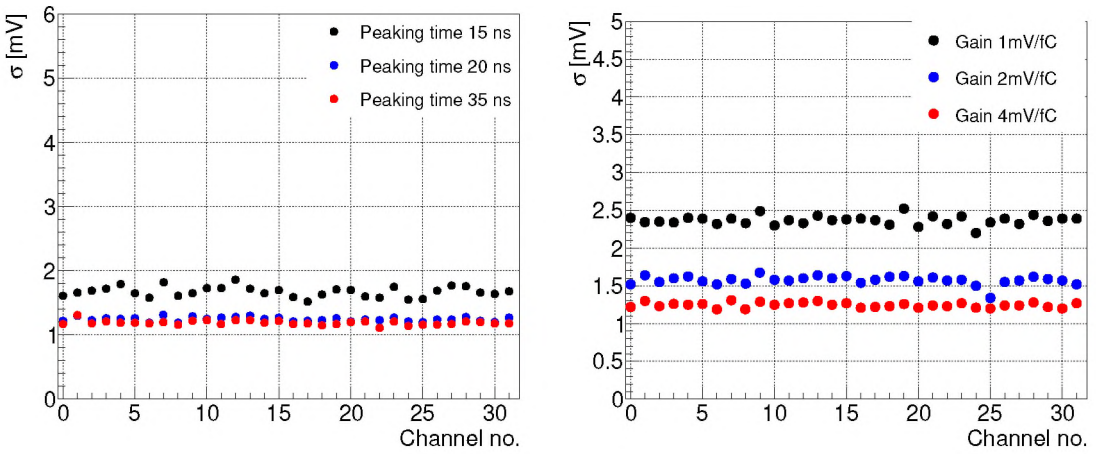


Figure 4.32: Left: Noise in PASTTREC channels calculated using the s-curve method for peaking-times 15 ns, 20 ns and 35 ns. Right: Noise in PASTTREC channels calculated using the s-curve method for gain set to 1 mV/fC, 2 mV/fC and 4 mV/fC. Noise is observed to be decreasing with the increase in the gain.

and the TOT spectrum was compared. The TOT measured for various gain and detector high-voltages is shown in Figure 4.33. The TOT at 1650 V and gain of 4 mV/fC is similar to the 1800 V and gain of 1 mV/fC.

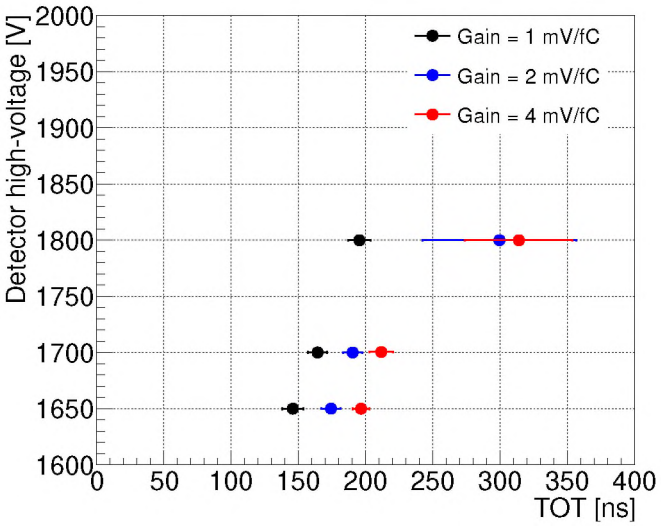


Figure 4.33: TOT calculated for varying detector high-voltages and PASTTREC gain set to 1 mV/fC, 2 mV/fC and 4 mV/fC.

The HADES FT detector (STS1+STS2) was constructed in 2020. The detector was tested extensively under lab conditions and later installed at HADES in 2020. It was later tested under a proton beam of momenta 3 GeV/c at the HADES pre-commissioning beam-time in 2021. The drift-time and TOT were compared for these gain and detector high-voltages using the FT in these beam conditions. The drift-time and the TOT spectra are observed to be identical for the PASTTREC gain of 1 mV/fC (at 1800 V), 2 mV/fC (at 1740 V) and 4 mV/fC (at 1650 V), as shown in Figure 4.34. Hence, reducing the high voltage and increasing the gain

should not affect the time and energy resolution of the detector. Instead, reducing the detector's high voltage by 100 V (1800V to 1700 V) will increase the lifetime of the detector under radiation by two times (slower ageing).

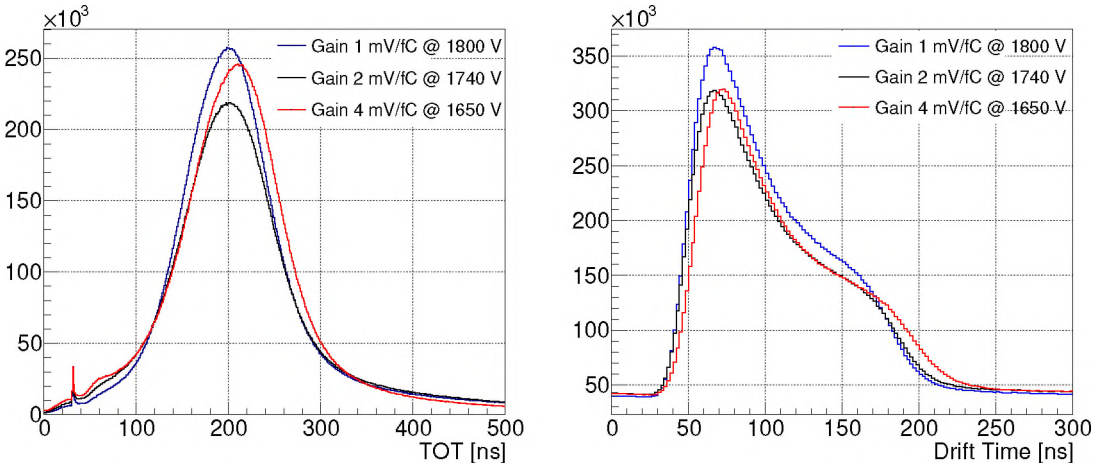


Figure 4.34: Left: TOT calculated from FT detector at HADES at gain 1 mV/fC, 2 mV/fC and 4 mV/fC and detector high-voltage set to 1800 V 1740 V and 1650 V respectively. Right: Drift-time calculated from FT detector at HADES at gain 1 mV/fC, 2 mV/fC and 4 mV/fC and detector high-voltage set to 1800 V, 1740 V and 1650 V, respectively. The TOT and drift-time for all three configurations present similar behaviour.

Selected operational parameters

The spatial resolution and detection efficiency improve with the increase in the detector's high voltage, and the ageing-effect increases. The energy resolution improves with the increase of the discriminator threshold, but the spatial resolution and the detection efficiency will decrease. The energy resolution improves with the peaking-time, but the electronic noise in the PASTTREC channels increases, and the spatial resolution degrades. An increase in gain allows for a decrease in HV and achieves the same performance as at reduced HV, hence reducing ageing, All the observations made in this chapter are summarised in Table 4.4. The set of parameters that can provide a balanced overall performance is selected for FT operation and presented in Table 4.5.

Table 4.4: General trend in detector performance with the increase in the operational parameters of the detector and PASTTREC.

Increase of	Noise (lower is better)	Spatial resolution (lower is better)	Energy resolution (higher is better)	Det.Efficiency (higher is better)	Aging (lower is better)
HV	-	Higher	-	Higher	Higher
Threshold	-	Lower	Higher	Lower	-
PT	Higher	Higher	Higher	No.Conc	-
Gain	Lower	-	-	-	lower

Table 4.5: Selected operational parameters

Detector high-voltage	1700 V
Gain	4 mV/fC
Threshold	10 mV (STS1), 20 mV (STS2)
Peaking-time	20 ns
TC-setting	setting2

4.5 FT at HADES p+p (4.5 GeV) experiment

A dedicated Forward Detector was constructed to extend the acceptance of the HADES Spectrometer towards lower polar angles, 0.5° – 6.5°. This detection system consists of two FT stations, a high-precision time-of-flight wall based on RPC technology and a high-granularity scintillator-based hodoscope. As this detector operates in a field-free region, particle identification has to be performed based on dE/dx and time-of-flight measurements. The straw tube tracking stations (STS) are also used to reconstruct off-vertex decays. The first FT station (STS1) was built by the Nuclear Physics Institute, Forschungszentrum, Jülich, Germany and the second FT station were built by the Marian Smoluchowski Institute of Nuclear Physics, Jagiellonian University, Kraków, Poland. STS1 has 704 straw tubes of length 76 cm arranged in four double layers arranged in 0°, 90°, 90°, 0°, inclination to the vertical axis, respectively. It has a beam opening of 8 × 8 cm^2 at the centre. STS2 has 1024 straw tubes of length 125 cm arranged in four double layers arranged in 0°, 90°, 45°, -45°, inclination to the vertical axis, respectively. It has a beam opening of 16 × 16 cm^2 at the centre. The STS1 and STS2 are placed at 3.1 and 4.6 m, respectively, downstream of the target. The Forward Detector system installed at HADES is shown in Figure 4.35.

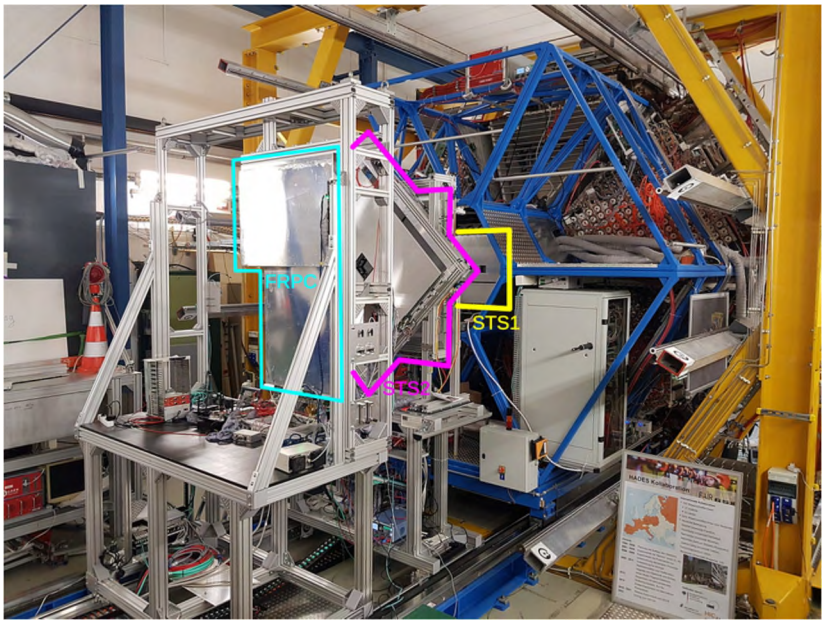


Figure 4.35: Forward Detector system installed at HADES. Two straw tube FT stations STS1 and STS2.

A production beam-time to study p + p collisions at Ekin = 4.5 GeV was conducted at HADES (maximal SIS18 energy). Over 41 billion events were collected in 488 hours of data taking (684 TByte), at an average event rate of 40 - 55 kHz in four weeks (February/March 2022). The FT experienced rates up to 2×10^5 per straw. The FT was configured with the operational parameters chosen based on the studies presented earlier in this chapter (Table 4.5). The operation of the FT under the beam was stable and successful as :

- All FT straws (704 + 1024) were operational.
- No detector high-voltage breakdowns.
- Stable operation of the gas system.
- Stable operation of all PASTTREC FEBs (44+64), no breakdowns.
- Stable operation of FT TRB read-out system.

After the detector was installed at the HADES beam-line, a noise scan was performed using the parameters described in 4.5. The obtained noise width (σ) and the distribution of baseline position for STS2 FEBs is shown in Figure 4.36. The noise level is observed to be well below the operational threshold (≈6 times).

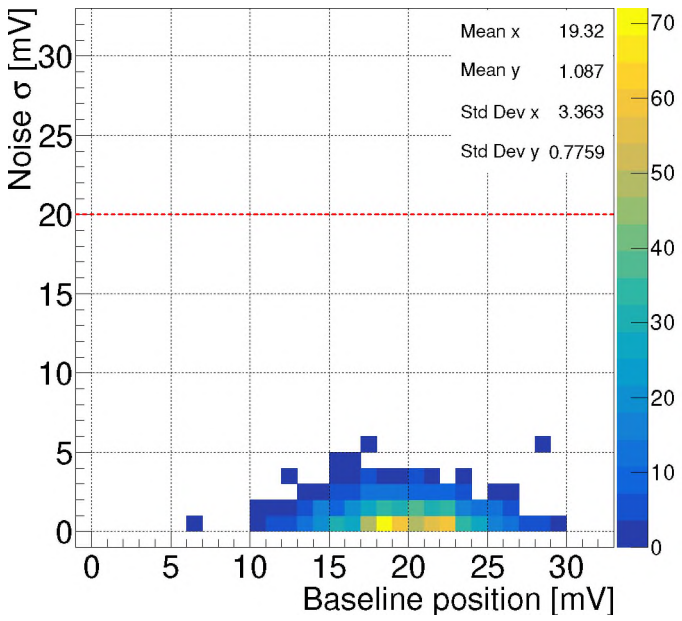


Figure 4.36: Noise width (σ) and baseline position obtained from noise scan performed on STS2 FEBs (1024 channels). The discrimination threshold level is indicated in a dotted line (red).

The raw drift-time and TOT spectra collected (before straw-wise space-time calibrations) from the FT under beam operations are shown in Figure 4.37 and Figure 4.38. The uniformity in DT and TOT among all the channels of both detectors is a result of the studies presented in this chapter.

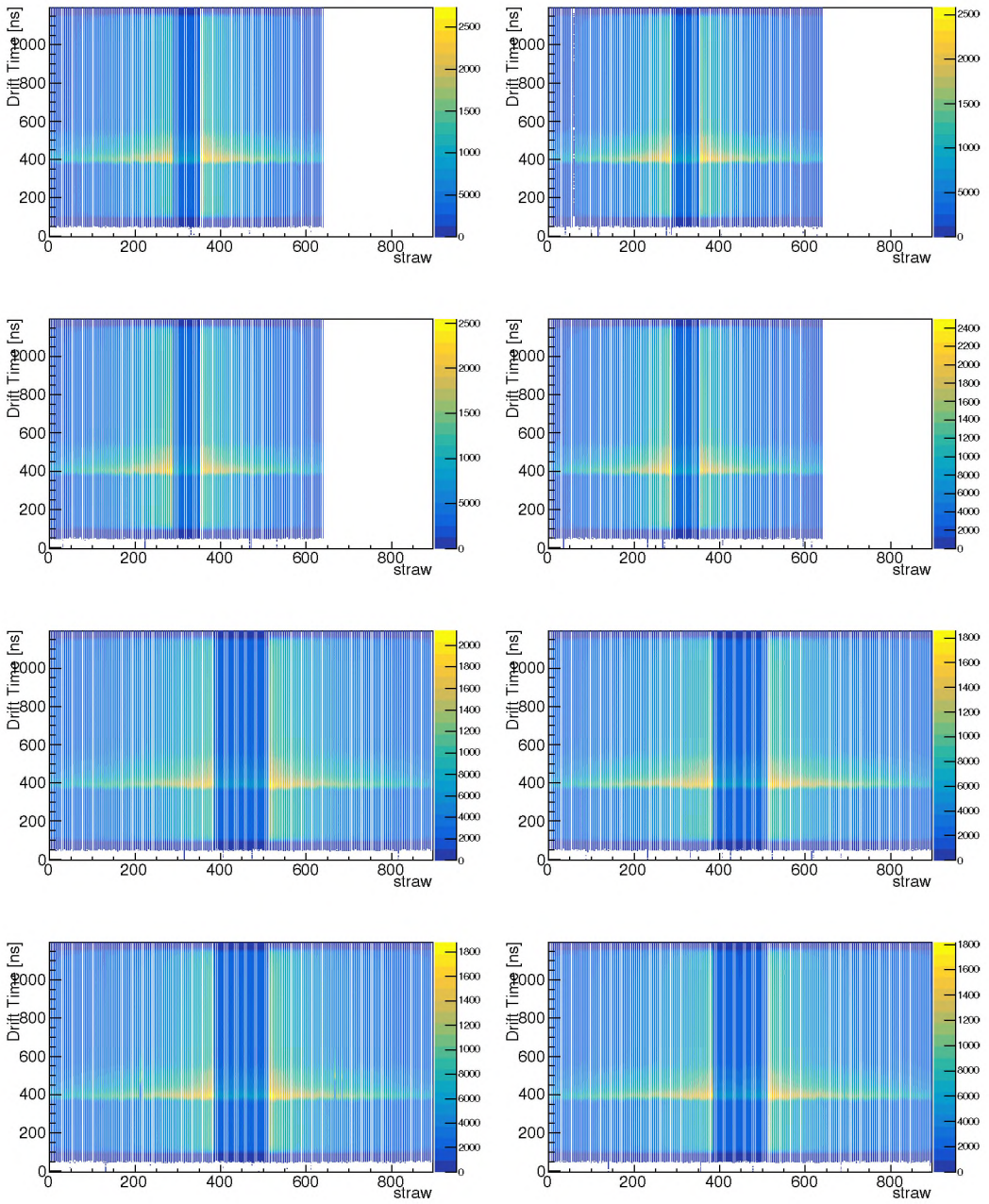


Figure 4.37: Raw drift-time spectra from STS1 and STS2 double layers (4 + 4) at HADES.

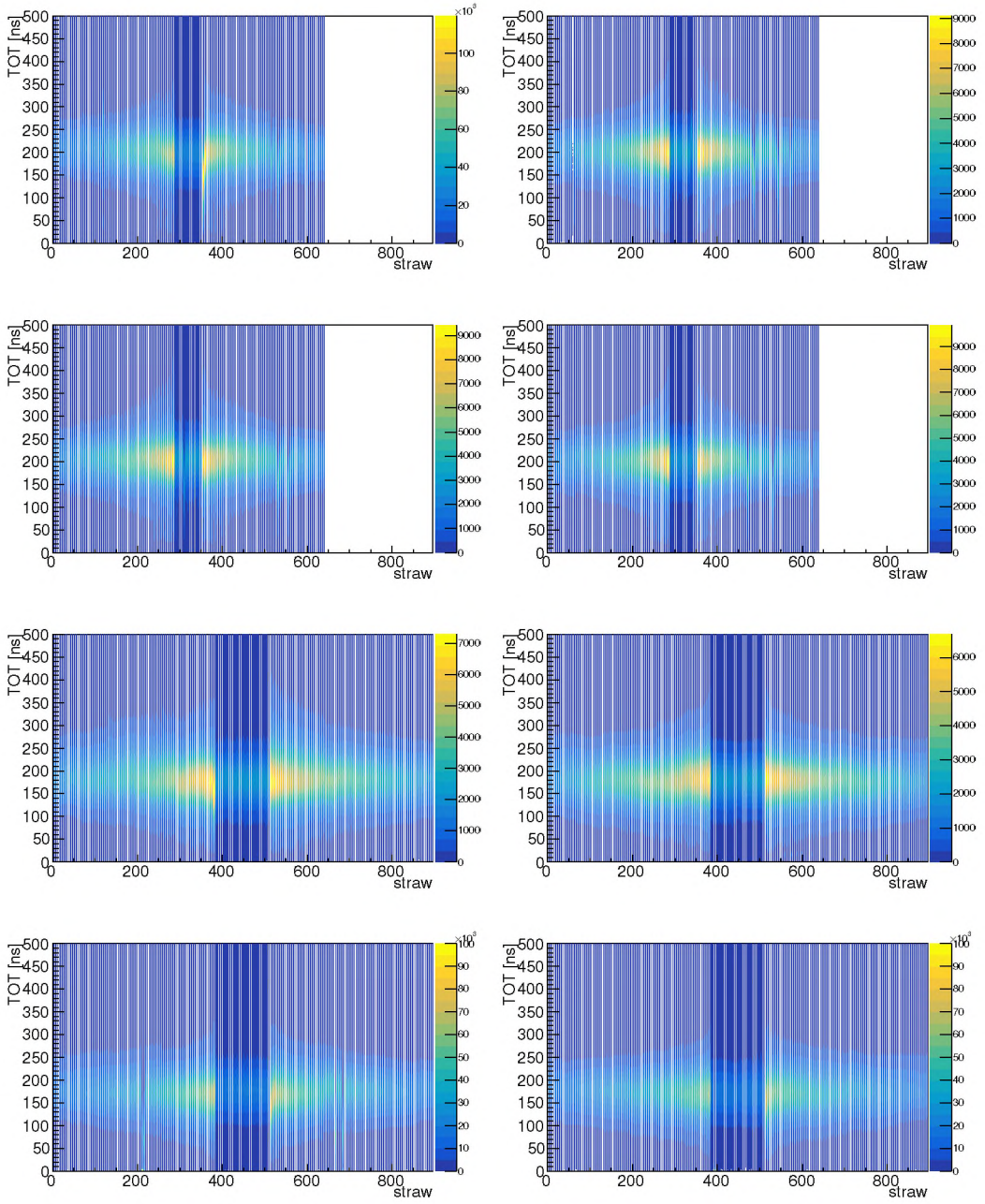


Figure 4.38: TOT spectra from STS1 and STS2 double layers (4 + 4) at HADES.

The pp-elastic scatterings were measured by reconstructing the proton pairs from the HADES-FD and the preliminary results are available. In an elastic scattering of two particles, the energy and momenta of the reaction are conserved and the vector sum of all momenta particles taking part in the reaction is 0. As a result, the resultant protons in pp-elastic scattering are co-planer. The difference in the φ angle between the resultant protons w.r.t the beam is equal to $\Delta\varphi$ 180°. The tangent product of the polar angles of the outgoing protons (θ_1 and θ_2) is a constant as described in equation 4.9.

$$\tan\theta_1 \tan\theta_2 = \frac{1}{\gamma_{cm}^2} \tag{4.9}$$

Where γ_{cm} is the Lorentz-factor ($\frac{1}{\sqrt{1-\frac{v^2}{c^2}}}$) in the centre-of-mass system. Similarly, the momentum of the outgoing protons can be calculated as a function of their polar angles.

$$p_1 = \frac{p_{01}}{\cos(\theta_1)[1+\tan^2(\theta_1)\gamma_{cm}^2]} \tag{4.10}$$

Where p_{01} is the incident beam momenta and θ_1 is the polar angle of the outgoing proton of which the momenta is being calculated.

Based on these kinematic constraints, the pp-elastic events from the p+p @ 4.5 GeV experiment at HADES are reconstructed. A selection of these reconstructed pp-elastics was later performed using the following conditions:

- $\tan\theta_1 \cdot \tan\theta_2 = 0.29429 \pm 0.1$ (calculated based on beam energy).
- Co-planarity of the reconstructed protons has to be in the range $173° < \Delta\varphi < 187°$.
- Difference in the measured momenta w.r.t the theoretical momenta calculated using equation 4.10 has to be $\Delta p \pm 500$ MeV.

The tangent product of the scattering angles and the co-planarity of the reconstructed pp-elastic protons from the experiment is presented in Figure 4.39 (right) in comparison to the simulation studies (left).

The number of reconstructed pp-elastics N^{pp} from the $\Delta\varphi$ peak (Figure 4.39) and selected using the conditions described above are used to calculate the integrated accepted luminosity of the experiment using equation 2.3 described in Chapter 2. The pp-elastic reconstruction efficiency $\varepsilon_{el,sim}$ using HADES-FD is $\approx$ 80% and the total reconstruction efficiency w.r.t 4π solid-angle is estimated to be $\approx$ 43%.

The integrated accepted luminosity calculated for the p+p @ 4.5 GeV experiment at HADES using the pp-elastics reconstructed from the HADES and FD reached $\sim$ 5.9 pb^{-1} as shown in Figure 4.40.

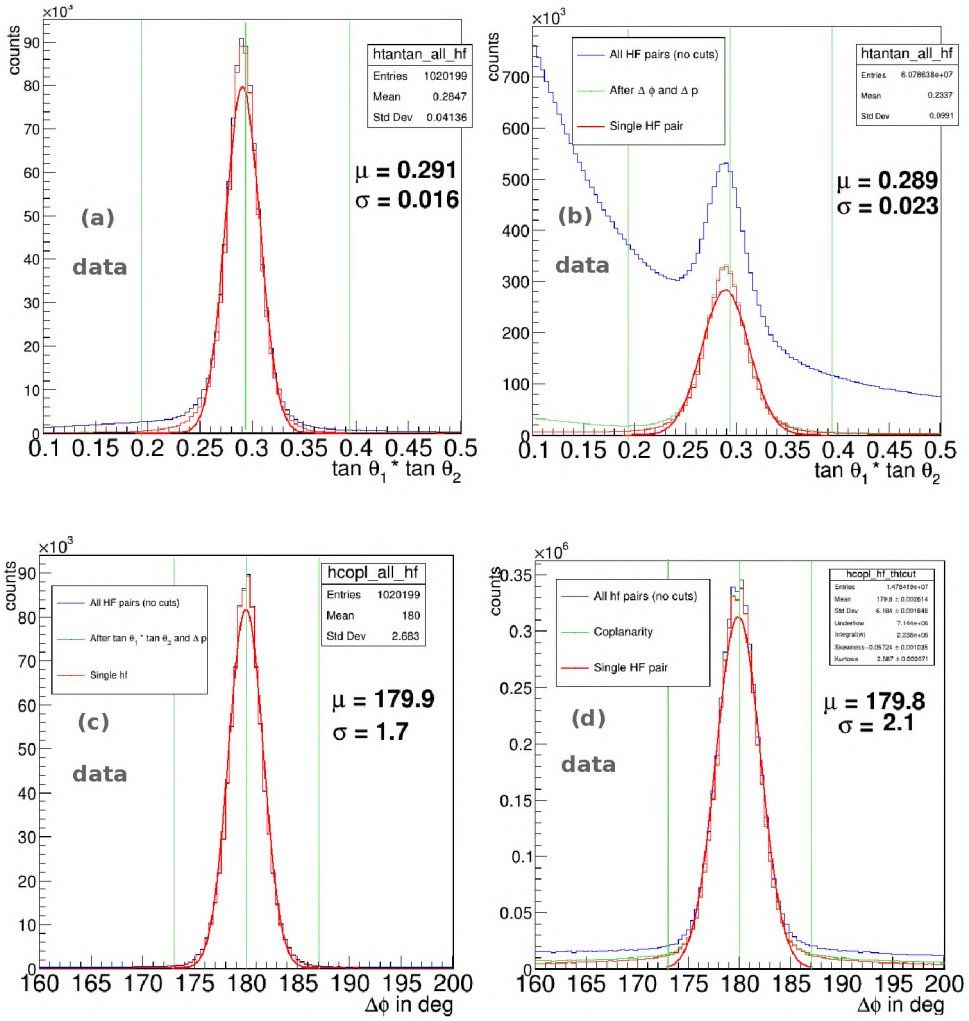


Figure 4.39: (a) The tangent product of the polar angles of the pp-elastic outgoing protons obtained from simulation studies. (b) The tangent product of the polar angles of the reconstructed pp-elastic outgoing protons obtained from data. (c) $\Delta\varphi$ of the pp-elastic outgoing protons obtained from simulation studies. (b) $\Delta\varphi$ of the reconstructed pp-elastic outgoing protons obtained from data. The histograms are presented for simulations and data before any selection (blue), after the selections on the tangent product of polar angles and co-planarity (green) and on added selection on momentum difference (red) as described above. This analysis was done by the HADES physics working group.

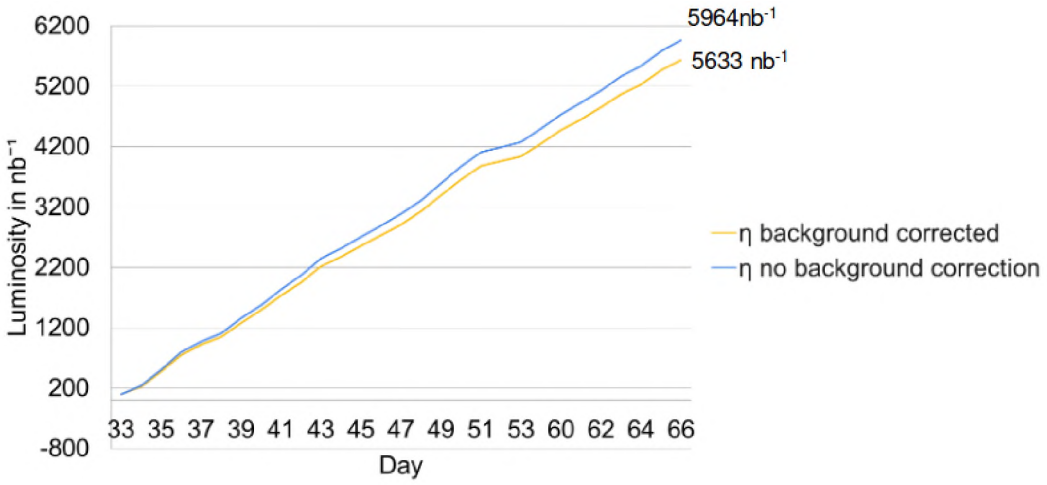


Figure 4.40: Integrated luminosity calculated for p+p@4.5 GeV experiment at HADES using the yields obtained in the pp-elastic $\Delta\varphi$ peak.

Chapter 5

Real-time data processing for FT

The $\overline{\text{P}}$ANDA experiment will not use fixed hardware triggers; instead, the event selection is based on real-time feature extraction, filtering, and high-level correlations. A firmware framework for such real-time data processing has been developed and tested with hardware setup for a $\overline{\text{P}}$ANDA Forward Tracker prototype. The solution is applicable for other detector subsystems based on the TRB data read-out system.

The $\overline{\text{P}}$ANDA experiment will operate at high beam-target interaction rates reaching 20 MHz [10], with a wide variety of events topologies and a dedicated list of features to distinguish and identify interesting physics processes. Consequently, data collection generates a continuous data stream of about 200 GB/s [3]. The continuous read-out allows for more flexible measurements but also gathers excess data, even when no hits are detected in some subsystems. For instance, the Forward Tracker (FT) can produce from 1 GB/s to 10 GB/s depending on the $\overline{\text{P}}$ANDA mode of operation [4, 31]. This large amount of raw data could be significantly reduced in the initial stages of the Data Acquisition System (DAQ).

As described in Chapter 2, 'FEE' is a section of the DAQ that uses custom hardware which is common to all $\overline{\text{P}}$ANDA subsystems and should operate in a real-time regime. The network infrastructure transmits digitised data from all the $\overline{\text{P}}$ANDA subsystems. The data packets belonging to the same time frame are sent to a single OPN for further online analysis. The OPN will perform processing of complete time frames from all the subsystems using various algorithms implemented in CPU and GPUs. It is therefore important to reduce the size of the raw data stream at the Data Concentrator level by filtration and extraction of useful information only.

As $\overline{\text{P}}$ANDA operates under continuous read-out mode, feature extraction will be used for data reduction. A data processing pipeline for such feature extraction has been developed and has been adapted successfully in the read-out for the $\overline{\text{P}}$ANDA FT detector prototype. As the hardware for the final $\overline{\text{P}}$ANDA DC is still under development, the processing pipeline has been implemented and tested on a commercially available board, Xilinx ZCU102, which is equipped with a Zynq UltraScale+ MPSoC. The system and the processing algorithm and some of the obtained results are presented in this chapter.

5.0.1 System Requirements

The $\overline{\text{P}}$ANDA FT consists of 12,224 straws arranged in three pairs of tracking stations: one pair (FT1, FT2) is placed before the dipole magnet, the second pair (FT3,

FT4) inside the dipole magnet, and the third pair (FT5, FT6) is placed after the magnet. It will use the TRB5sc, the latest hardware of the TRB family [32]. Each TRB5sc provides 64 TDC channels, sufficient to read-out 4 FEBs, and 9 TRB5sc boards will be mounted on a custom crate. Each crate will house a master board which acts as an interface between the slave TRBs in the crate and the DC, as shown in Figure 5.1. The DC will function as a bridge between the output of the master board and the network infrastructure. The data in the DC are stamped with time information, synchronized and are read-out to the network infrastructure at a rate defined by the SODANet (see further). The proposed intermediate pre-processing pipeline in the DC has to unify the data streams from master boards arriving at the DC and filter the data before they are sent over to the network.

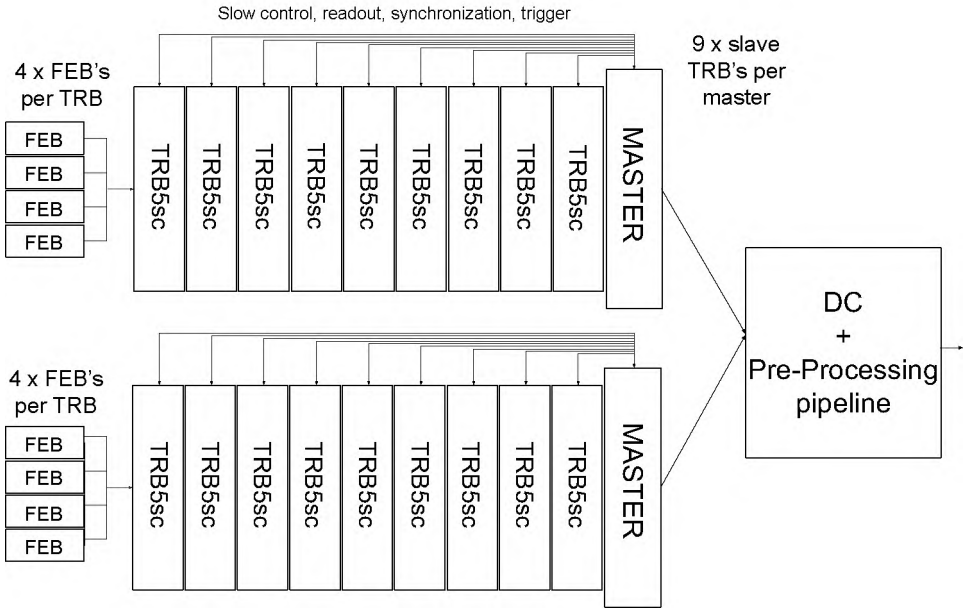


Figure 5.1: Schematic view of the TRB5sc system for the Forward Tracker read-out. Four FEBs (analogue FEE) are connected to a TRB5sc (digital FEE) with a ≈10 meter long 40-pin ribbon cable. A master board interfaces 9 TRBs placed in a crate to the DC hardware.

Table 5.1: $\overline{\text{P}}$ANDA-FT read-out requirements and projected data rates.

	FT 1,2	FT 3,4	FT 5,6
No. of channels	2304	3328	6592
Average hit rate per straw	35 kHits/s	31 kHits/s	9 kHits/s
TRB5sc's	36	52	103
Master boards	4	6	12
Total bandwidth	324 MB/s	410 MB/s	237 MB/s

The number of TRB5sc, master boards and expected data rates for each of the $\overline{\text{P}}$ANDA FT station pairs are presented in Table 5.1. The pre-processing pipeline must be compact enough to be implemented on the FPGA that will be used in the DC hardware (Xilinx Ultrascale+ KU15P) and guarantee to filter the data from all the links without compromising any valuable information.

In the $\overline{\text{P}}$ANDA experiment, the interaction of the antiproton beam with the internal proton target will last for 2 μs and will be followed by an interval of 400 ns. This interval is used to gain time for the data processing. Such a 2.4 μs cycle is called a burst, and 16 such bursts make up one 'super-burst'. Detector data are read out from the DC on each super-burst update, i.e. at ~26 kHz (SODANet frequency) [3]. The pre-processing pipeline has to be capable of filtering the data within this time limit (~38.4 μs). Additionally, as DC is a common system for all detectors in $\overline{\text{P}}$ANDA, the pre-processing pipeline is expected to be easily adapted by other detector systems using TRB-based read-out or other read-out hardware that use similar data formats.

5.1 Pre-processing pipeline

5.1.1 General Layout

The developed processing pipeline is designed to be placed within the DC firmware, in between the data receivers from the detector subsystems and the common network. The data are received, prepared for processing, analysed for feature extraction by the processing component, prepared for transmission, and transmitted in a push-forward manner as shown in Figure 5.2. The extracted feature can be either used as a parameter to filter out meaningless data from the stream (packet validity) or can be transmitted as an additional data packet along with the original data. It is designed to mimic the software analysis stages described in Section 4.3. The user can decide how the data have to be handled in the pipeline. The three modes of operation of the designed module that can be selected are listed below.

- Filtering mode: Only the filtered data packets with meaningful features are transmitted, and the raw data from the TRB and the data packets with no interesting features are dropped, thus reducing the data volumes.
- Marking mode: All the raw data from the TRB is transmitted, and the data packets with meaningful features are marked with a header word, thus preserving the raw data for further analysis. This mode allows estimating the effect of filtering via offline analysis.
- Bypass: Raw data from the TRB links are forwarded out to the network without any pre-processing.

The pre-processing unit has a modular structure, and the components share a common, simple interface that is described in Table 5.2.

The communication modules in the processing pipeline implement a basic set of network protocols (ARP, DHCP, ICMP, IP, UDP) that allow to directly connect the TRB Ethernet output links to the pre-processing pipeline over the Gigabit transceivers (Xilinx GTH). The module accepts the data from all the TRB boards and forwards them along with the Start-Of-Packet (SOP), End-Of-Packet (EOP), and Data-Valid (DV) signals for the preparation of the data in the pipeline.

Data from different links can arrive at different times and can have different packet sizes. The data packets are stored in de-randomisation buffers until the data from all the links (EOP) arrive and a single, parallel data stream is constructed.

Table 5.2: Pre-processing pipeline-interface with the TRB inputs, user inputs and pipeline outputs.

	Name	Description
System	SYSCLK_IN	Clock input from Clock manager (default 200MHz)
	RESET_IN	Global reset on startup from the Clock manager
TRB inputs	TRB_DATA_IN	Data input from receiver module (8-bits per link)
	TRB_SOP_IN	Start Of Packet (SOP) signal from the receiver module(1-bit per link)
	TRB_EOP_IN	End Of Packet (EOP) signal from the receiver module(1-bit per link)
	TRB_DV_IN	Data Valid (DV) indicating the Active duration of the data signal from the receiver module (1-bit per link)
User inputs	USR_UDP_IN	UDP port ID for the outgoing data packet (16-bit per link)
	USR_MODE_IN	Processing mode select (user input)
Pipeline outputs	FD_DATA_OUT	Data output to the transmitter (32-bits per link)
	FD_SOP_OUT	Start Of Packet signal to transmitter module (1-bit per link)
	FD_EOP_OUT	End Of Packet (EOP) signal to transmitter module (1-bit per link)
	FD_DV_OUT	Data Valid (DV) indicating the Active duration of the data signal to the transmitter module (1-bit per link)

These data are then mirrored into two separate data paths: one preserves the original raw data, and the other one is used for applying the processing and filtering mechanisms. They are both synchronised in time to react to the processing results, e.g. drop, forward or mark the current data packet upon feature extraction decision.

The processing component is the module in the pipeline which is dedicated to the extraction of the features from the data. The Features extracted by the processing unit are of two kinds: the event classification feature and a derived feature. The event classification feature is used for zero suppression by resolving the validity of the data packet after checking it across user-defined conditions. The derived feature is the meaningful information generated additionally after analysing the zero-suppressed data. All detector-specific operations and algorithms are performed here, and this component can be easily replaced to serve other applications. With modern technologies like High-Level Synthesis (HLS) [33], complex detector-specific analysis can be made simple and adapted in this module, as long as the pipeline's interface and timing are maintained. HLS allows to accelerate development and debug cycles of the algorithmic and computational parts of the pipeline through their implementation in C++ and then conversion to regular HDL components. This also enables the direct reuse of source code used in the offline analysis, ensuring consistency. The raw TRB data, filtered data from the processing component, and the features extracted all arrive at the preparation stage for transmission. Depending upon the operation 'mode' (USR_MODE), the data (FD_DATA) to be transmitted is packed and transmitted to the designated destination (USR_UDP).

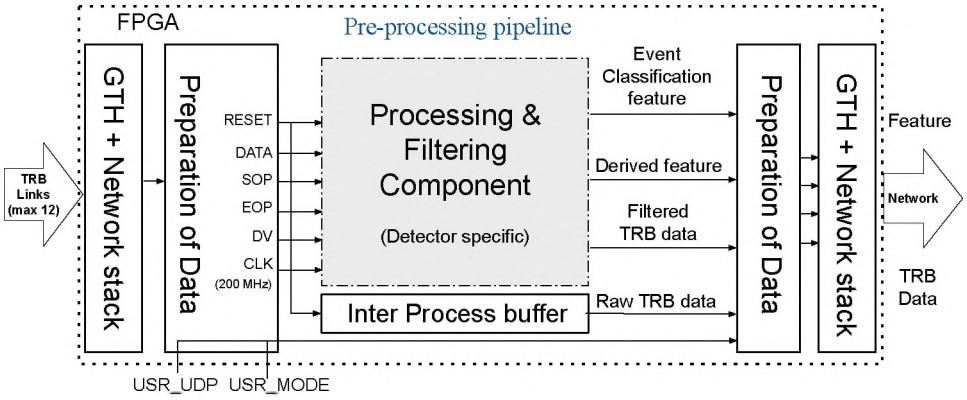


Figure 5.2: Scheme of the processing components and pre-processing pipeline. The layout represents the components of the system implemented in the FPGA. It consists of a transceiver network stack, data preparation modules, inter-process buffers and the data processing and filtering component (see text for details).

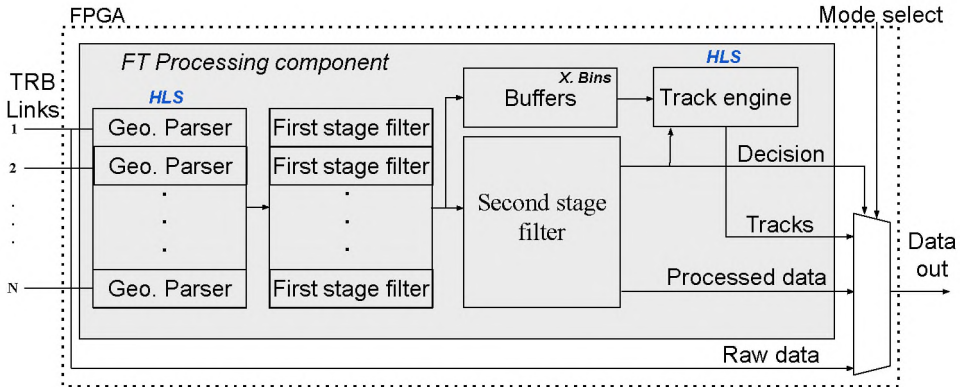


Figure 5.3: Schematic view of the component of the processing pipeline for the FT with the geometry parser, first stage filter, second stage filter and the tracking engine (see text for details).

5.1.2 Pre-processing for FT

The task of the FT in $\overline{\text{P}}$ANDA is the reconstruction of particle trajectories. Therefore, the key information to be extracted from the data stream is the identification of data packets with tracks and their parameters. Being able to identify data packets with valid tracks originating from the target will eliminate background induced from 'out-of-the-target' interactions.

In the context of this work, the time duration between two read-outs is called a time frame. It can contain many interaction events with multiple tracks. Additionally, the straw tubes are slow detectors with a maximum drift-time of 180 ns. In order to identify and separate these tracks, the time and TDC channel information transferred from the TRB must be translated into hits in the detector geometry, sorted in time order of signal arrival, and later checked across the track recovery conditions so that accidental coincidences are discarded. The analysis module of FT data is made of four components displayed in Figure 5.3: Geometry parser, first-stage filter, second-stage filter, and tracking engine. These are described in detail below.

5.1.3 Geometry Parser

The Geometry Parser is the first module in the 'FT processing component'. The data received by the pre-processing unit are prepared for processing and forwarded to the geometry parser. A lookup table describing the relation between the TDC channel and the detector geometry is provided to the parser. In this way, the data are stamped with the geometry parameters like detector layer, module, straw and its coordinates (x, y, and z) in the global reference system, which will further be necessary for reconstructing tracks from data. The processing is parallelised by a dedicated instance of geometry parser for each of the input links (TRB crate) in the processing component. This module is implemented using HLS, as it entirely relies on the detector geometry and could be modified easily for any change in the detector setup.

5.1.4 First Stage Filter

The first-stage filter assures the quality of the raw data. The raw data may consist of packets with no hits (empty packets), hits with minor glitches (noise), or corrupted, i.e. TDC artefacts. This includes hits with repeated edges (rising or trailing), missing time-stamps, or unrealistic TOT. Such data words can produce fake multiplicities, thus affecting the track reconstruction conditions in the further stages. The role of the first-stage filter is to reject such data. Firstly, a 64-bit word is constructed by utilising the calibration and geometry attributes from the geometry parser, as described in Table 5.3.

Table 5.3: Data format for FT processing component

Bits	Attribute
0	Pair valid flag
1	LT pair check flag
2	Epoch time corrupt flag
3	Hit valid flag
4	Rising-Falling edge
5 - 10	Straw
11 - 14	Straw layer
15 - 18	Detector Module
19 - 50	TDC Time
51 - 63	Unused

Every data word arriving at the first-stage filter module with a rising edge waits for the next word in a shift register. The data word is pushed forward only if the next word is a trailing-edge. This ensures to have a rising and falling edge pair and mitigates the risk of having fake hits. In order to eliminate corrupted hits, the time stamp in the data word is compared with the reference time of the associated TDC, and the data are accepted only if the difference is within a reasonable range. An instance of the first-stage filter is created for every input link in the system.

5.1.5 Second Stage Filter

In a continuous read-out mode, the data units represent time-frames of fixed length. Particle tracks can be extracted from a pool of hits only after sorting them into well-separated groups inside a given time period corresponding to the physical event. For this purpose, the entire time-frame is divided into smaller time-bins, and all the hits in the time-frame are sorted into these time-bins based on the rising edge of the respective hit. These time-bins are treated individually from here on, and the presence of a potential track can be recognised if the time-bin fulfils the following configurable coincidence conditions:

- Number of hits in a time-bin must be above the minimum number of hits required to reconstruct a track.
- Hits must be present in defined layers of the detector.
- Hits in a time-bin must be in pairs for a defined number of detector layers (FT straw layers consist of two staggered straw planes).

With all these conditions fulfilled, the group of hits in this time-bin is defined to originate from the same event and constitutes a track.

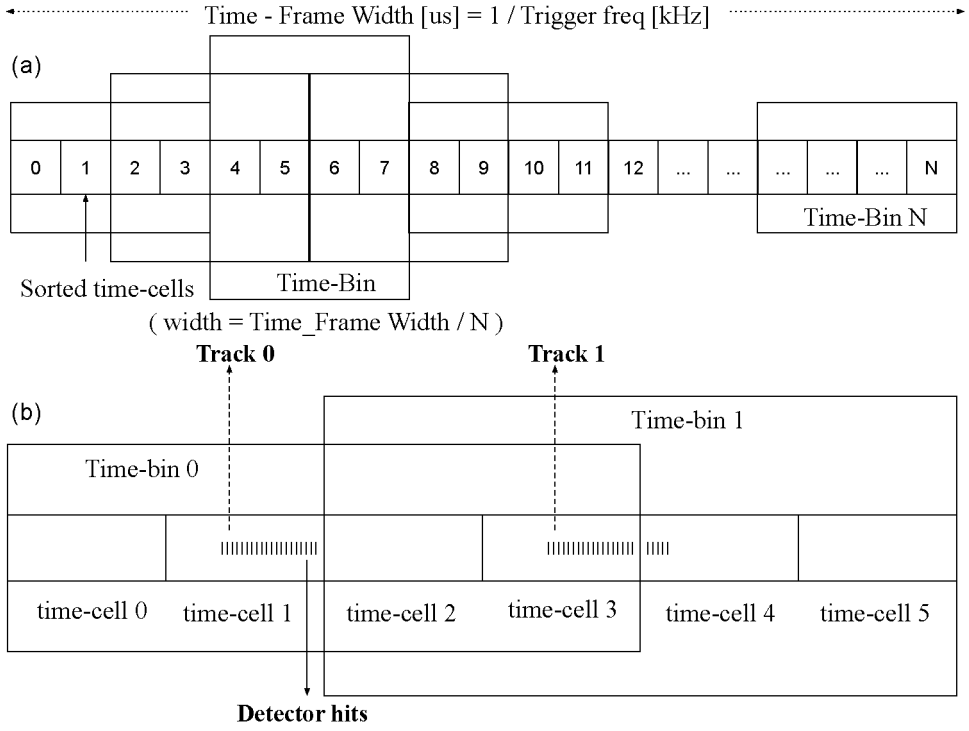


Figure 5.4: Schematic representation of a time-frame divided into 'N' number of time-bins consisting of four time-cells each (a). Schematic illustration of a case with more than one track in a time-bin. 'Track 1' is separated from 'time-bin 0' to 'time-bin 1' due to the overlap of time-cells (b).

These virtual time-bins must be large enough to capture all the hits belonging to a track and small enough to avoid mixing of tracks. To achieve this task, each time-bin is further divided into four 'time-cells' of suitable width, into which the hits

will be assigned based on its TDC rising time as shown in Figure 5.4. The number of time-bins per time-frame depends strictly on the time-frame length, drift-time of straws (≈ 180 ns), and the resources available in the pre-processing hardware.

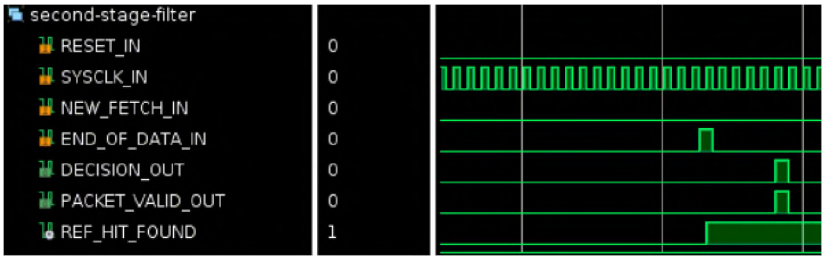


Figure 5.5: Waveform diagram from the FPGA simulations of second stage filter. The end of the data packet in a time-frame is represented by' END OF DATA IN' (EOP). The completion of the coincidence search is indicated by the 'DECISION OUT', and the time-frame is flagged as a potential track event by the 'PACKET VALID OUT' signal within six clock cycles after the EOP.

To avoid the hits belonging to a track being spread across adjacent time-bins, they are overlapped by two time-cell units. With this, we can expect all the hits from a track to be in a common time-bin and can be checked for the track recovery conditions. When all the filtering conditions are satisfied, the time-frame is recognised to be valid, and a positive decision is issued from the second-stage filter along with the index of the time-bin containing the potential track. The sorting of hits into the time-bins and the coincidence checks are done in a push-forward manner as the data passes through the component. The decision on the presence of a potential track is issued five clock cycles after the last data word (EOP) in the time-frame has arrived (for a total of 25 ns in the hardware used). The width of the time-cells, the number of time-bins per time-frame, the overlap offset, and the coincidence conditions in this stage are configurable and can be tuned based on the operational conditions of the detector.

5.1.6 Tracking Engine

A copy of the data supplied to the 'second-stage filter' is buffered when the data are processed for feature extraction (see Figure 5.5). The index of these buffers is equivalent to the index of the time-bins in the second-stage filter. On the arrival of a positive decision and the index of the time-bin with potential tracks from the second-stage filter, the tracking engine reads data from the respective buffers. The tracking engine is an HLS component written in C++ capable of performing a simple reconstruction of tracks (low-resolution tracking as done in the software Section 4.3.5) in 2D space based on the position of anodes in the vertical straw layers (no drift-time information is used). In the first stage, hits in every detector layer are grouped into 'clusters' and 'hit-pairs'. A 'cluster' is a group of hits in an individual straw layer, while a 'pair' is a set of two neighbouring straws in a cluster. The ambiguity in track position is later solved by selecting the combination of these hit-pairs with the least χ^2 obtained from the linear fit. The parameters of this track are the derived feature from the data and are described by a 64-bit word. Multiple tracks in a time-frame can be simultaneously reconstructed by using an

instance of the tracking engine for every time-bin. This tracking component for the FT data consists of loops and inline functions required to solve the combinations. The number of track combinations to solve in a time-bin can vary. Due to this, the component has a variable latency of ≈6 μs. As the tracks appearing in a time-frame are sorted into time-bins, a tracking engine interfacing these time-bins has abundant time (length of the time-frame) to complete the task until another track appears in the same time-bin in the upcoming time-frames.

5.1.7 Resource Usage

The processing pipeline has been developed, keeping in mind the scalability of the system. The resources required to implement the pipeline entirely depend on the number of data links required in the detector read-out. An instance of all the components in the processing pipeline is dedicated to each input link except for the common processing and filtering component. Projected resource consumption of a processing pipeline with 12 TRB links (FT 5,6) for both the evaluation ZCU102 board and the FPGA in the targeted DC hardware (Kintex UltraScale+ KU15P) are presented in Table 5.4.

Table 5.4: Resource consumption

Component	Block RAM Blocks	CLB LUTs	DSP Slices
Available in DC (KU15P)	984	522,720	1,968
Available in (MPSoC ZCU102)	912	274,080	2,520
Receiver, Clocks, Geo-parser, first-stage filter, buffers, transmitter (for 12 links)	846	106,500	1512
Processing component (second-stage filter)	0.0	8565	0.00
Track buffers + tracking engine	0.5	9624	6

5.1.8 Test Scheme

A generic testing and development scheme has been realised for the evaluation of the pre-processing system. The raw data to be processed can be streamed to the processing module directly from the TRB via GbE links but requires an active detector and the DAQ system ready for operation. An alternative approach is to convert the pre-collected raw data from the TRB to the adequate binary format and stream it to the pre-processing module to mimic the data from the detector. In both cases, the processed data output and the features extracted by the module are sent back to the PC. The same raw data can be analysed by the offline analysis software to benchmark the performance of the processing module by comparing the results. It can also be sent to the FPGA simulator for further development of the pre-processing components under realistic conditions, hence completing the entire development and testing cycle.

5.2 Evaluation of the system

The quality of the features extracted by the module could be evaluated by comparing the data processed by the hardware against the results obtained using offline software data analysis tools as described in Section 5.1.8. For this purpose, the pre-processing pipeline has been extensively tested with the data streams from in-beam experiments and radioactive sources obtained with detector prototypes. For the test of the system under beam conditions, the detector prototype (described below) was exposed to proton beams with momenta of 3 GeV/c and with a peak intensity of ≈20 kHz at the COSY, Forschungszentrum Jülich (Germany) accelerator facility in early 2019. The data to be processed can be streamed to the processing module directly from the TRB links via GbE links but requires an active detector and DAQ system ready for operation. An alternative approach is to convert the pre-collected data from the TRB or from other hardware platforms into binary with software tools and stream it to the pre-processing module to mimic the data from the detector. In both cases, the processed data output and the feature extracted by the module are streamed back to the PC storage as shown in Figure 5.6. The same raw data could be analysed by the offline analysis software to benchmark the performance of the processing module by comparing the results. The same raw data could also be streamed to the FPGA simulator for the further development of the pre-processing components under realistic conditions, hence completing the full development and testing cycle.

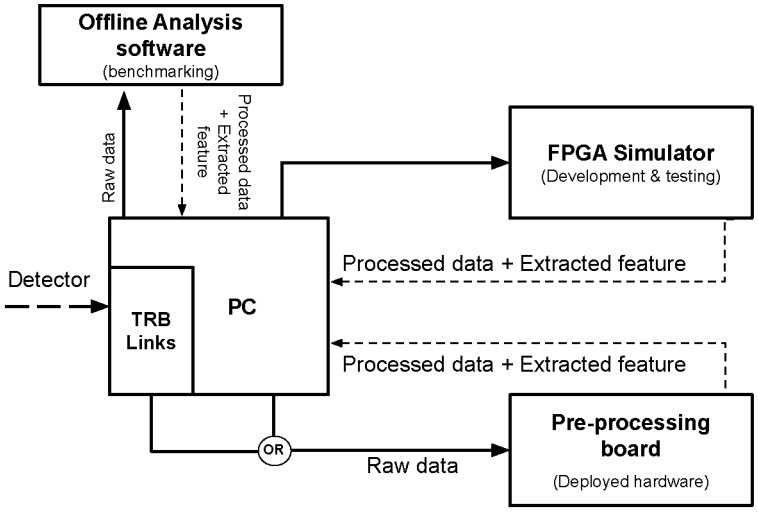


Figure 5.6: Schematic representation of the testing and developing platform for bench-marking the performance of the pre-processing module.

5.2.1 Test setup: Detector and readout

The FT prototype used in tests was built with eight double layers of straws of length 125 cm, each having one module i.e. 32 straws. The layers were arranged in 0°, 5°, -5°, 0°, 0°, 5°, -5°, 0° inclination to the vertical axis respectively. A 7.5 × 7.5 cm^2 wide plastic scintillator detector was placed before the straw modules and was used for the reference time (T0)[34].

The TRBv3-based master-slave architecture was used to read-out the detector FEBs as the TRB5sc hardware was in the stage of development during this period.

A master TRBv3 with the Central Trigger System (CTS) [17, 20] firmware was used to emulate SODANet time-frames for the two slave TRBv3. One of the slave TRBv3 contains four 48-channel TDCs. The second TRBv3 contains three 48-channel TDCs and an FPGA configured to read out scintillator signals. The collected data were sent to the Zynq UltraScale+ MPSoC ZCU102 hardware configured with the pre-processing pipeline using a Gigabit Ethernet (GbE). The read-out system is shown in Figure 5.7. The output links of the pre-processing hardware were connected to the event-builder PC to store the data and control the system. The detector was read out in a continuous mode with time-frames of 50μs, and the processing component was configured with 127 time-bins of width 1.2μs each (320 ns per time-cell). The track parameters extracted by the pre-processing pipeline were stored in the same PC and were synchronised with the raw TRB data using the trigger number.

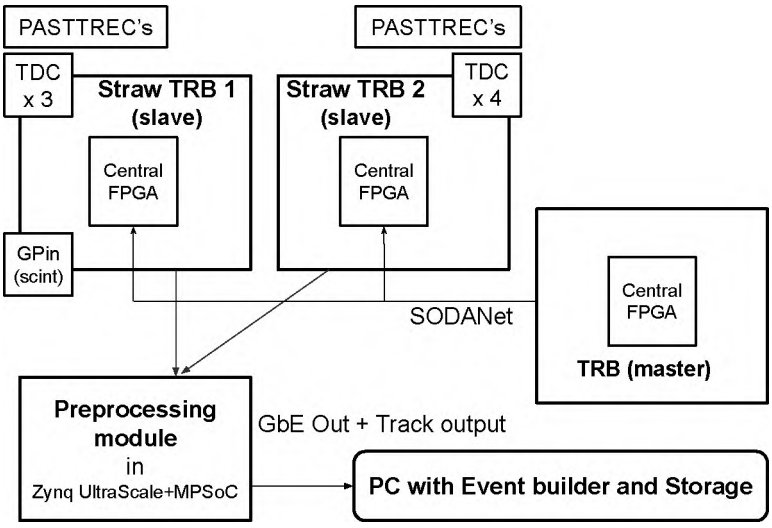


Figure 5.7: A schematic representation of the DAQ for the test setup showing the connection between PASTTREC front-end-boards, TRB and pre-processing board.

5.2.2 Results

The processing system identifies the time-frame that contains tracks and filters out the non-track time-frame. The pre-processing pipeline stage was operated in the "marking mode", marking the time-frame containing tracks while retaining all the other time-frames in the data output. This allowed us to compare these marked and unmarked time-frames with the track reconstruction performed by the offline analysis. In an ideal case, all the time-frames from which the tracks are extracted by the offline analysis must be marked by the pre-processing pipeline, and the excess marking of time-frames due to wrong identification must be zero.

The collected data contained 3.9 million time-frames. They were analysed by the offline software, and tracks were reconstructed from 23.07% of these time-frames. When the same data was streamed through the pre-processing pipeline, 25.54% out of the 3.9 million time-frames were marked by the hardware as potential track frames. Over 99% of time-frames found in the offline analysis are also marked by the pre-processing hardware. Less than 0.01% of the time-frames were not marked by the hardware due to the errors in the TDC that corrupted a single data word

in the stream, resulting in the rejection of this hit belonging to the track in the first-stage filter, but could be recovered in the software analysis. A surplus of 2.47% of time-frames not found by the offline analysis was marked by the hardware, as it does a more lenient analysis of the data compared to the offline (example: stricter time-coincidence with the reference detector). This marking efficiency of over 99% proves the track recognition capability of the pre-processing pipeline. Being able to efficiently extract this information from the data stream in real-time will prevent all the meaningless data from entering the network.

The system was also tested with detector data from radioactive sources and cosmic rays. The pre-processing hardware was streamed with data directly from the detector read-out, and the marking efficiency remained the same, proving the system's stability irrespective of the source from which the data are streamed.

The data reduction capability of the pre-processing system depends entirely on the environment (mainly radiation intensity) to which the detector is subject. For the conditions in which the system was tested, around 74.54% of time-frames were rejected when the detector was exposed to the proton beam and over 99% were rejected when exposed to radioactive source/cosmic rays due to empty frames. The rejected data for trackless time-frames are mostly empty data packets with the essential header and data from a few co-incidental detector hits. These data packets still constitute 35% of the data volume in the case of the beam data and over 99% in the case of radioactive source/cosmic rays.

The second feature extracted (derived feature) from the data using the tracking engine in the pre-processing pipeline (hardware), i.e. the parameters of the track are compared with the one obtained from the offline analysis (software). The tracks were straight lines ($y = mx + C$) inside the detector geometry, and the calculated track parameters (offset and the slope) of these tracks for both offline and hardware-based track reconstruction are presented in Figure 5.8 and Figure 5.9. The track parameters presented for tests of the system under cosmic rays cover a larger angular range as expected. The parameters of the track show a very high agreement between the software and hardware-based tracking for both perpendicular and inclined tracks, as seen in the difference plot (Figure 5.10). The slight difference observed in the parameters of the track is due to accidental coincidences that the tracking engine implemented in hardware could not resolve. This can be mitigated by narrowing the width of the time-bin and introducing additional filtering conditions. As the efficiency of the system is adequate, streaming just the extracted features instead of both data and the feature would significantly reduce the data volume in the future.

These track parameters can be also used to determine the origin of a particle track in an experimental setup. By using this selection, only data for the tracks originating from the interaction vertex can be accepted, and the rest (i.e. secondaries) of the data can be rejected from entering the network. This feature of the FT pre-processing pipeline can also serve as a platform for the visualisation of the data in real-time and online monitoring during the experiments. This is an excellent example of a system that requires complex computing, like solving combinations being easily and effectively implemented on FPGA using technologies like HLS.

Additionally, T0 and drift-time (DT) are the two features that are important for the analysis of the data in the further stages of the DAQ. The mean rising time of all the hits in a track can be treated as T0 after some offset subtraction and can be used to calculate the DT. Tests of the detector under beam conditions show that the

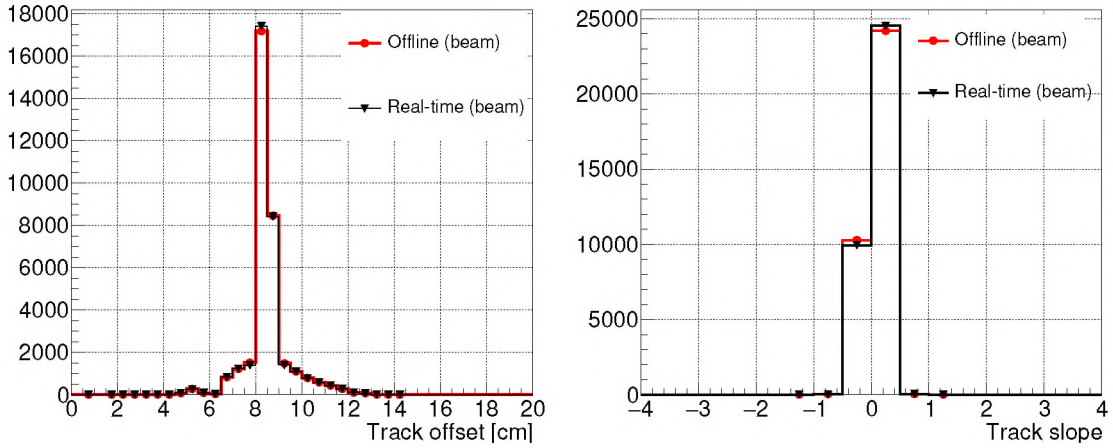


Figure 5.8: The parameters of the tracks obtained from in-beam measurements. Left: Distribution of the track offset (C) for the tracks reconstructed using offline software analysis for the in-beam data (red), using real-time pre-processing for the in-beam data (black). Right: Distribution of the track slope (m) for the tracks reconstructed using offline software analysis for the in-beam data (black), using real-time pre-processing for the in-beam data (red).

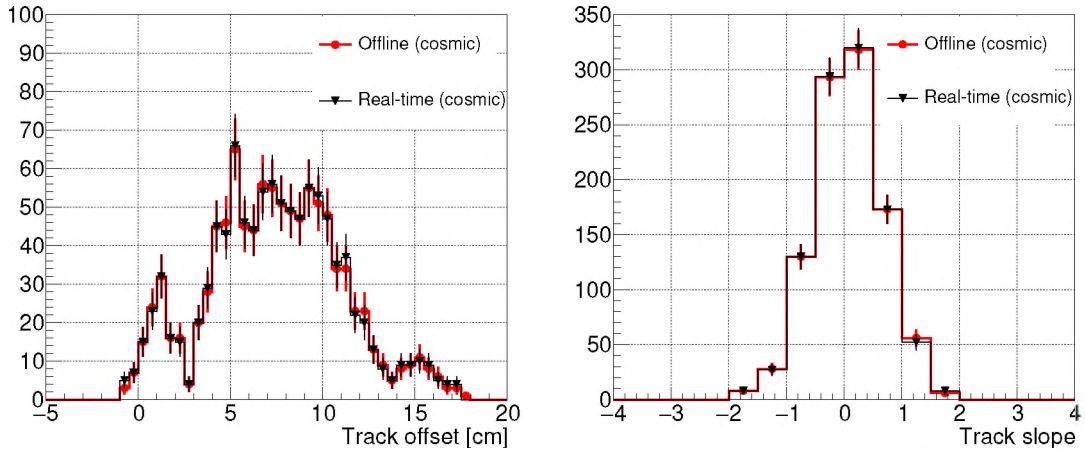


Figure 5.9: The parameters of the tracks obtained from radioactive/cosmic ray measurements. Left: Distribution of the track offset (C) for the tracks reconstructed using offline software analysis for the radioactive/cosmic ray data (red), using real-time pre-processing for the in-beam data (black). Right: Distribution of the track slope (m) for the tracks reconstructed using offline software analysis for the radioactive/cosmic ray data (black), using real-time pre-processing for the in-beam data (red).

DT calculated using this method is similar to the value obtained using a reference detector like a scintillation detector, as shown in Figure 5.11. This information can be extracted instantaneously in the second-stage filter stage of pre-processing. All these results can collectively make up a self-reliant read-out that can provide the OPN with refined FT data.

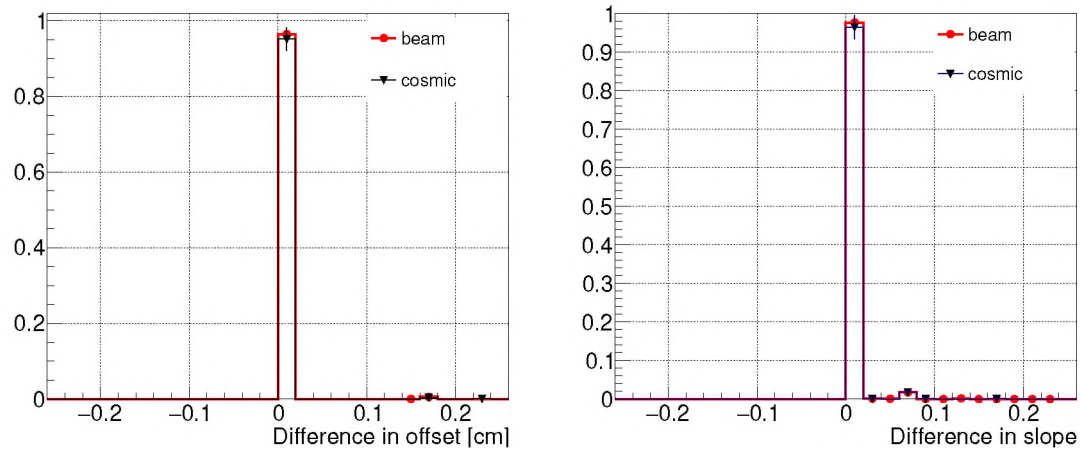


Figure 5.10: Left: Difference between offline and real-time values of offset (C). Right: Difference between offline and real-time values of slope (m)

5.3 Optimisation prospects

The time measurement component in the TRB produces a 32-bit word for every hit in the detector containing channel number, rising time (relative to the super-burst update time), and TOT [35]. With the super-burst update frequency of 26 kHz (time-frame width = 38.46 μs), it requires at least 17 bits (0.5 ns/bit) to represent the rising time of a hit. Rather than transmitting the rising time for every hit in an event, it is sufficient to transmit a single reference time (T0) for an event and the rising time of the hit with respect to this T0, which is also the DT. DT is a small number (≈180 ns) that can be represented in 9 bits (1 bit = 0.5 ns), allowing a hit to be represented in just 24 bits. This encoding would reduce the input data rate of the FT by 25%. Due to the efficient isolation of events in the time-bins of the second-stage filter, T0 and DT can be easily obtained.

Furthermore, Straw Tube Tracker (STT) will be another detector in $\overline{\text{P}}$ANDA, constructed using similar straws and read-out components, that can benefit from this pre-processing pipeline.

From simulation studies for $\overline{\text{P}}$ANDA, it is known that tracks from secondary particles produced by the interaction of particles with the elements of the $\overline{\text{P}}$ANDA detection system amount to 1.5 times the primary tracks [10]. The goal is to reject these tracks. The average time distance between hits in FT from two events is ≈200 ns (High-Resolution Mode). As the hits are sorted into the time-bins, by instantiating multiple tracking engines, multiple tracks in a time-frame can be reconstructed simultaneously. The reduction in data rates due to the rejection of tracks from secondary interactions is expected to be significant. Furthermore, the features extracted from the pre-processing pipeline (T0, DT, and track parameters) can be stored in some buffer to be later utilised by the OPN. They will reduce the time required for synchronous processing. The project's future development includes the development of a tracking engine capable of reconstructing tracks in 3D space and studying the data reduction by rejecting secondary tracks.

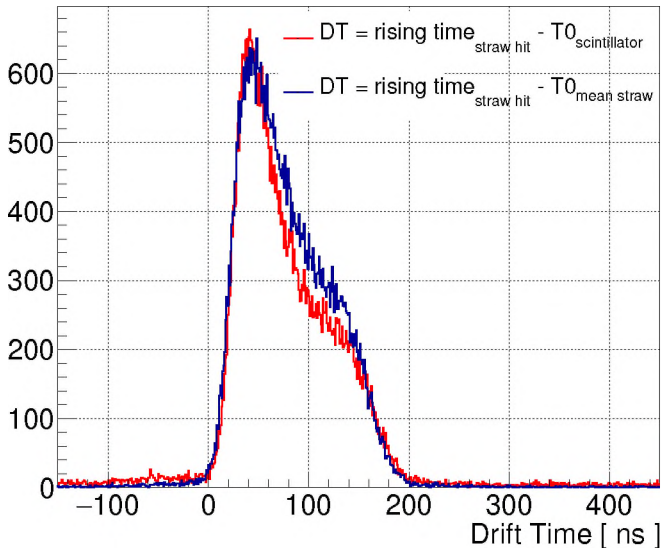


Figure 5.11: Drift time (DT) calculated using the reference time T0 from a scintillation detector placed behind the FT (blue) compared to the DT calculated using the mean rising time of the hits in a track (red) in the offline analysis, presented after offset correction.

Chapter 6

Summary and Outlook

The work presented in this thesis focused on the development of the readout and data acquisition system for the Forward Tracker (FT) of the upcoming $\overline{\text{P}}$ANDA experiment with prior tests in the FT prototype setup at COSY and at the upgrade of the HADES experiment. The work has been presented in two parts: The detector and readout calibration methods are discussed in Chapter 3, Chapter 4 and the developments towards the FT DAQ are discussed in Chapter 5. Laboratory testing was carried out for both parts to investigate the developments, and in-beam tests were then used to evaluate and confirm the results.

6.1 Discussion of Results

Gain and baseline homogeneity are two of the PASTTREC's most crucial variables. The PASTTREC's high gain uniformity enables treatment of all channels equally without the need for separate calibration processes for leading-time and TOT. To achieve this uniformity, the baseline levels of all channels, which vary due to the intricate manufacturing process, must be re-aligned after power-up. The other important factor is the intrinsic noise in the PASTTREC channels. Reducing the noise levels in the channels not only improves the signal-to-noise ratio but also allows us to increase the amplification gain and reduce the detector's high-voltage, further increasing the detector's lifetime. It has been shown that it is possible to assess if a particular channel is suitable for operation based on the noise level and its proximity to the threshold at the 0 mV point.

In order to find such baseline positions and noise levels, two methods have been investigated: S-curve measurement and the noise profile scan. During both procedures, the baseline or threshold of each channel in the chip is shifted, and the number of registered output pulses is measured at each step. Despite the fact that the S-curve approach delivers accurate data on baseline position and noise levels in the PASTTREC channel, its time requirements and requirement for an external pulse generator make it impractical to employ on a large detector setup. It was proven that the developed noise-scan method was a reliable tool for the qualification of the FEBs. The qualification scheme for selecting the FEBs and the TC configurations for the PASTTREC FEB, mainly by measuring the baseline uniformity and noise profile was presented. This methodology was used to select the FEBs and the settings for the FT detectors in the HADES experiment (STS1 and STS2 in p+p @ 4.5 GeV, 1728 channels in total). This procedure will be further used to select the

FEBs for the STS and FT detectors in the $\overline{\text{P}}$ANDA experiment.

Other aspects of this work include quantifying the key detector performance factors, identifying the influencing parameters, and assessing their impact on the performance of the detector. In order to study the noise in the FEBs, tracking resolution, energy resolution, detection efficiency, and detector ageing for various PASTTREC (threshold, gain, and TC settings) and high-voltage configurations, an FT prototype detector was tested under beam conditions. The software tools and the calibration methods required to analyse the detector data were developed and the following results were obtained:

- The data collected in beam conditions made it possible to estimate the detector efficiency for various detector high-voltages. The detection efficiency of the detector ranges from 94% at 1650 V to 98% at 1850 V. These results suggest that detection efficiency can be enhanced by increasing the amplification gain in the PASTTRECs instead of increasing the high-voltage on the detector.

- The spatial resolution obtained from reconstructing 3 GeV proton tracks varied between 170 μm to 300 μm in dependence on the detector's high-voltage and threshold level. The obtained results suggested discriminating the signals at lower thresholds (or increasing the gain) would improve the tracking resolution of the detector.

- The data collected has allowed for the investigation of the PID capability of the straws by using the TOT information. Truncated mean TOT was calculated from FT tracks (8 hits) and the separation power for various high-voltage and PASTTREC configurations were obtained. It has been observed that threshold position in the PASTTRECs can strongly influence the separation power. Too low a threshold decreases separation power but increases detector efficiency and TOT resolution.

- The average noise in PASTTREC channels is σ <1.5 mV/fC (at amplification 4 mV/fC). This is five sigmas below the standard operation threshold (20 mV). It is an important observation as it indicates the scope for reducing the threshold in the FT.

- The tests conducted have proven that drift-time and TOT spectra are identical for the PASTTREC gain of 1 mV/fC (at 1800 V), 2 mV/fC (at 1740 V) and 4 mV/fC (at 1650 V), as shown in Figure 4.33. Reducing the high-voltage and increasing the gain should not affect the time and energy resolution of the detector. Instead, reducing the detector's high voltage by 100 V (1800 V to 1700 V) will increase the lifetime of the detector under radiation by two times.

Based on this study, it was possible to realise the influence of different operating parameters on the detector performance and arrive at a balanced configuration for FT. The best performance was obtained at Detector high-voltage: 1700 V, amplification gain: 4 mV/fC, discriminator threshold= 20 mV, peaking-time: 20 ns, TC setting: TC_{C1} = 10.5pF, TC_{R1} = 27kΩ, TC_{C2} = 0.9pF, TC_{R2} = 20kΩ. This configuration was for the FT at the p+p @ 4.5 GeV experiment at HADES. The FT data from this experiment was used for the reconstruction of the pp-elastic scattering events and for the luminosity determination. The study of hyperon resonances is

currently an ongoing process in the HADES physics analysis groups and the results of this study are expected to be published in the coming days.

The $\overline{\text{P}}$ANDA experiment will not use fixed hardware triggers; instead, the event selection is based on real-time feature extraction, filtering, and high-level correlations. In the second part of this work, a firmware framework for such real-time data processing was developed and successfully adapted in the read-out for the $\overline{\text{P}}$ANDA FT detector prototype. The processing pipeline was implemented and tested on a commercially available, Xilinx FPGA ZCU102, equipped with a Zynq UltraScale+MPSoC. Important features of the processing algorithm and some of the obtained results are described in Chapter 5 and summarized below:

- The developed processing pipeline was capable of unifying multiple data streams arriving from the TRBs, performing geometric calibrations, identifying and filtering corrupt data from the stream and performing time-based hit sorting in real-time. The components developed here will become a necessary part of a detector DAQ in $\overline{\text{P}}$ANDA if the detector data has to be processed online.

- The developed processing pipeline can perform multiplicity checks on detector hits and perform zero suppression. In the tests conducted with the processing pipeline connected to the detector readout, around 74.54% of data volume was reduced when the detector was exposed to the proton beam and over 99% when exposed to radioactive sources/cosmic rays. The rejected data for trackless time-frames are mostly empty data packets with the essential header and data from a few co-incidental detectors hits. It is also important to note that there was no accidental rejection leading to the loss of valuable data from the stream.

- The feature-extraction component of the processing pipeline has presented a very good track reconstruction capability. The parameters of the track show an agreement of over 99% between the software and hardware-based tracking for both perpendicular and inclined tracks in the FT. This efficiency of the system will allow streaming just the extracted features instead of both data and the feature would significantly reduce the data volume in the future. Collectively, a scheme to make up a self-reliant read-out that can provide the network with refined FT data and a reduction of 25% in data volume was presented.

The presented processing pipeline provides a promising concept of a fully integrated solution for FT and STT detector data processing in real-time. The $\overline{\text{P}}$ANDA experiment will use TRB-based read-out in several detector systems and the DAQ architecture has been designed keeping in mind the online and real-time data processing requisites. As the described pipeline is modular and expandable, it presents a high potential for use in TRB-based readout systems, in $\overline{\text{P}}$ANDA or in other experiments. The development of complex computing and data processing on SoC devices will assist the real-time particle tracking, event filtering, data reduction, and online monitoring for the FT in the future. The pre-processing pipeline will be an essential and easily adaptable extension of the TRB ecosystem performing data processing essential for both the DAQ and the end-user of the data.

6.2 Outlook

The FEBs with PASTTRECs and Trigger Readout Board (TRB) has been chosen as the base platform for the construction of the readout and data acquisition for the central tracker (4636 straws) and forward tracker (12224 straws) in $\overline{\text{P}}$ANDA. The system based on PASTTRECv3 and TRBv3 has been successfully and thoroughly evaluated in this work and implemented in the HADES FT and is expected to be used in $\overline{\text{P}}$ANDA high-resolution mode (first phase) where the expected average hit rates per channel reach only up to 35 kHits/s. However, in $\overline{\text{P}}$ANDA high-luminosity mode (second phase) the expected average hit rates per channel reach 350 kHits/s. The main digitising platform (TRB) needs to be upgraded to handle such data rates.

More than 1050 PASTTREC FEBs will be employed by $\overline{\text{P}}$ANDA's straw tubes. These FEBs must be qualified and tested in accordance with the guidelines outlined in Section 3.4 and all of their configurations must be organized and saved in some way. These configurations contain settings for things like TC, baseline positions, and calibration factors like TOT-Gain characteristics for each channel, among others. Meanwhile, the $\overline{\text{P}}$ANDA central tracker's FEBs are organized in a small area. A potential issue could be the FEBs heating up due to the restricted airflow. For these reasons, the straw read-out will be improved by integrating a temperature sensor with chip ID functionality into the FEBs.

To address the necessary modifications, a solution involving TRB5sc as the digitizing platform and FEBs with a temperature sensor has been developed. The development consists of a new adapter (add-on) card between PASTTREC FEB and TRB5sc, and firmware and software updates required to adapt the hardware changes. The concept has been tested and described in Section A. Prototypes of all the modifications has be produced and further tested and finalised before the mass production of all the hardware required for the readout of $\overline{\text{P}}$ANDA straws. Furthermore, the data processing pipeline has to be extended and implemented on new hardware to extract features from the PANDA FT full system.

Appendix A

Upgrade of the FT read-out

All the key components of the FT read-out have been upgraded to an extent. The modifications in the hardware, firmware and slow-control software tools for the FT readout are described here.

A.1 PASTTREC FEB and the add-on card

The PASTTREC FEBs with packed ASIC are used instead of bonded ASICs. This will simplify the manufacturing process of the FEBs. A DS18S20 is chosen as the temperature sensor as shown in Figure A.1. It uses the OneWire interface for communication, which requires only one communication line. It consumes less power and as it derives power from the data line ("parasite power") — does not need a local power supply. It provides a 9 to 12–bit (select-able resolution) centigrade temperature and has a unique, 64-bit long serial number, providing board ID. Two PASTTREC ASICs, a KEL8930E-040 connector and the DS18s20 temperature sensor are mounted to a dedicated printed circuit board (PCB). The size of this PCB has been reduced to 5.3×5.6 cm (will benefit the space constraint in PANDA central tracker).

The communication between the FEB and the TRB platform requires an adapter (add-on) card that will drive and deliver the signals to the FPGA mounted on the TRB.

A dedicated add-on card has been designed, prototypes produced and evaluated. The card enables connection to 4 PASTTREC FEB and switching between PASTTREC ASICs and DS18520. The switching is performed by the assertion of a dedicated line, controlled by the FPGA firmware on the TRB. The add-on card connecting the FEB to the TRB5sc is equipped with a Samtec ERM8-75 connector in direction of TRB5SC and 4x KEL8930E-040 connectors in direction of the FEB. As PASTTREC's Chip-Select (CS) line is used for the reset, a dedicated set of data (MOSI) lines has been added. Single-ended lines are converted to differential lines using a CDCLVD1204 differential buffer. Additionally, another line is added for switching the communication between the DS1820 and the PASTTREC on the FEB using a 74LV4066 analogue switch. The schematic of the components connected together is presented in Figure A.2.

The schematics of the PASTTREC FEB and the PASTTREC FEB - TRB5sc adapter boards are included.

Figure A.1: A prototype FEB for FT read-out with bonded PASTTREC ASIC and DS18s20 temperature sensor mounted.

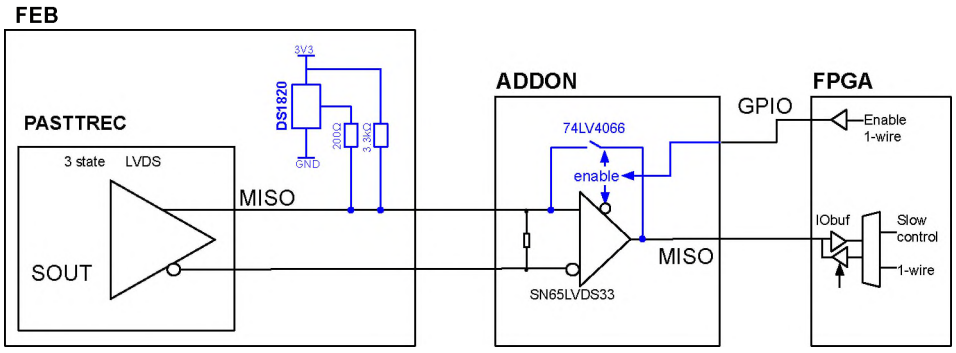


Figure A.2: Schematic of the connection between TRB5SC, addon and PASTTREC ASIC.

A.2 PASTTREC FEB interface with TRB5SC

Figure A.2 presents the connection of the PASTTREC ASIC and the DS1820 to the controlling FPGA located on the TRB5sc board through the add-on board with the MISO selection mechanism. Detailed pin-out of the TRB5SC and the add-on boards are described below in tables A.1 and A.2.

Table A.1: Description of the TRB5SC physical connections pinout

Name	pin	type	function
CS[3:0]	[B19, A19, C18, A18]	out LVCMOS25	Reset of PASTTREC
SCK	C5	out LVDS	SPI clock
MISO[3:0]	[D19, C19, F18, D18]	in/out LVTTL33	Data input line shared between PASTTREC and DS1820
MOSI	P5	out LVDS	SPI data output line
PASTTREC_TEMP_SW	A20	out LVCMOS25	Toggle between PASTTREC and DS1820

A.3 Firmware

The FPGA on TRB5SC acts as a man-in-the-middle in communication between the control PC and the front-end board through register read/write transactions. The network packets with appropriate messages are received by the trb_net16_hub component and are redirected to the trb_net16_regio component that implements

Table A.2: Description of the add-on board physical connections pinout

Name	ERM pin	KEL pin
CS[0]	J1[71]	JCABLE_CONN1[39, 40]
CS[1]	J1[73]	JCABLE_CONN2[39, 40]
CS[2]	J1[75]	JCABLE_CONN3[39, 40]
CS[3]	J1[77]	JCABLE_CONN4[39, 40]
SCK	J2[1,3]	JCABLE_CONN(4-1)[37, 38]
MISO[0]	J1[72]	JCABLE_CONN1[33, 34]
MISO[1]	J1[74]	JCABLE_CONN2[33, 34]
MISO[2]	J1[76]	JCABLE_CONN3[33, 34]
MISO[3]	J1[78]	JCABLE_CONN4[33, 34]
MOSI	J2[2,4]	JCABLE_CONN(4-1)[35, 36]
PASTTREC_TEMP_SW	J2[6]	NA

register access functionality. After proper reception of the control and monitoring message, it has to be converted into a transaction with the front-end board compliant with the appropriate protocol: modified SPI for accessing PASTTREC registers or OneWire for accessing the DS1820.

Below is the table A.3 with registered addresses and descriptions:

Table A.3: Description of control and monitoring registers on TRB5SC

Register name	address	description
PASTTREC_TEMP_SW	0x0023	Mode switch between PASTTREC (0x0) and DS1820 (0x1)
TEMP_ID	0x000a 0x000b	Temperature sensor Unique ID (0xa LSB)
TEMP_VALUE	0x0008	Temperature sensor temperature value (11'b MSB)
PASTTREC_CLOCK_TOGGLE	0xd416	Manual toggle of the clock line
PASTTREC_REG	0xd400	Access to PASTTREC register
PASTTREC_REG_EXEC	0xd411	Execute PASTTREC register command
PASTTREC_REG_READ	0xd412	Value of PASTTREC register
PASTTREC_RESET	0xd417	Reset PASTTREC (0x0), to be followed by 25 clock cycles

The MISO line is shared between the PASTTREC interface and the DS1820, hence it is also used with two different protocols: modified SPI and OneWire. They differ in electrical standards and the direction of bit exchange. Therefore, the FPGA pin is configured as bi-directional LVTTL33, a tri-state buffer. In Lattice FPGAs it is done by instantiating the BB primitive component (table A.4).

Table A.4: Description of the BB component

Port name	description
I	Logic input, set to '0'
B	Input/Output to pin, connect to HW MISO pin
O	Logic output, connect to miso logic line
T	Logic tri-state input, connect to OneWire controller output when in DS1820 mode, else to '1'

The interface to DS1820 is provided by the trb_net_onewire component that implements the OneWire protocol. When enabled, the state machine periodically

performs read operations of registers that hold temperature and unique ID according to protocol timing constraints (considering 100 MHz master clock). The user interface of the component is presented in table A.5. As the bi-directional buffer is instantiated externally in the top-level component, the trb_net_onewire component should be configured to use separated input and output lines.

Table A.5: Description of the trb_net_onewire component

Port name	Type	Direction and size	description
USE_TEMPERATURE_READOUT	generic	[0, 1]	Include readout of the temperature
PARASITIC_MODE	generic	[0, 1]	Input deserialization only
CLK_PERIOD	generic	integer	Master clock period in ns
USEINOUT	generic	[0, 1]	Use bi-directional data line
CLK	port	input	Master clock
RESET	port	input	Active high reset input
READOUT_ENABLE_IN	port	input	State machine enable
ONEWIRE	port	in/out	Bi-directions OneWire data line (agree with USEINOUT generic)
ONEWIRE_IN	port	input	Input only data line (agree with USEINOUT generic)
ONEWIRE_OUT	port	output	Output only data line (agree with USEINOUT generic)
MONITOR_OUT	port	output	Output of OneWire received, serialized data
DATA_OUT	port	output [15:0]	Deserialized received data output (for debug only)
ADDR_OUT	port	output [2:0]	Address output (for debug only)
WRITE_OUT	port	output	FSM Operation mode (for debug only)
TEMP_OUT	port	output [11:0]	Decoded temperature value
ID_OUT	port	output [63:0]	Decoded unique ID value
STAT	port	output [31:0]	Component status vector (for debug only)

A.4 Procedures

In order to ensure proper operation of the system, it is required that the control and monitoring registers in PASTTREC ASICs are accessible from the level of the control computer. The communication between the PC and the TRB5SC board is realized through the Ethernet network (including an additional TRB3 board as an interface) and TrbNet protocol. The communication between the TRB5SC board and the PASTTRECs is realized through dedicated hardware lines and a modified SPI protocol (described in dedicated reports).

All accesses to PASTTREC and DS1820 registers are performed from the control PC using the trbcmd command. In order to perform a specific operation, a sequence of trbcmd commands has to be issued. In the following examples, we assume the FPGA connected to PASTTREC has TrbNet address 0x6500. The data format of PASTTREC commands has been described in previous reports. The examples below present operations performed on a single FEB.

```
Usage: trbcmd [-h] [-f script-file] [-n number] [-s time] [-d level] [-H] [-D] [-V] <COMMAND>
Options:
  -h     give this help
  -f     execute commands given in script-file
  -n     repeat COMMAND number times, -1 = endless loop
  -s     only if running in -n mode, sleep time in ms
  -d     turn on Debugging Information
         level 1: TRB_Package debugging
         level 2: +FIFO debugging
  -H     hex-mode: all arguments will be interpreted as hexadecimal-numbers
  -D     dec-mode: display register values as decimal numbers
  -V     version number

Commands:
    r <trbaddress> <register>                          -> read register
    rt <trbaddress> <register>                         -> read register&TimeStamp
    w <trbaddress> <register> <data>                   -> write register
    rm <trbaddress> <register> <size> <mode>           -> read register-memory
    rmt <trbaddress> <register> <size> <mode>          -> read register-memory&
                                                          TimeStamp
    wm <trbaddress> <register> <mode> <file>           -> write to register-memory
                                                          from ASCII-file
                                                          ('-' = stdin)
```

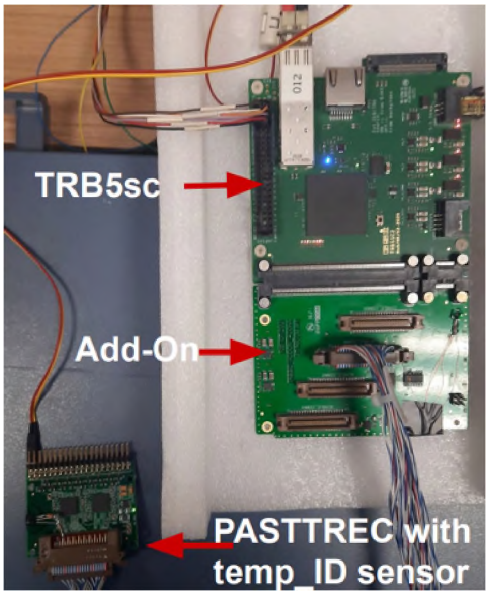


Figure A.3: Test setup constructed out of TRB5SC and add-on card with a connected PASTTREC FEB.

```
  i <trbaddress>                                    -> read unique ID
  s <uid> <endpoint> <trbaddress>                   -> set trb-address
  T <type> <random> <info> <number|%ctr>            -> send trigger
  TR <input> <type> <random> <info> <number|%ctr>   -> send trigger to RICH only
  I <type> <random> <info> <number|%ctr>            -> read IPU data
  setbit <trbaddress> <register> <bitmask>          -> set bits of a register
  clearbit <trbaddress> <register> <bitmask>        -> clear bits of a register
  loadbit <trbaddress> <register> <bitmask> <val>   -> load bits of a register
  nettrace <trbaddress>                             -> trace TRBNet-Path of an endpoint
  reload <trbaddress>                               -> reload FPGA
  reset                                             -> reset TRBNetwork
  comreset                                          -> reset Etrax-FIFO Logic
  f <channel>                                       -> flush FIFO of channel
  R <register>                                      -> read register of the FPGA
  W <register> <value>                              -> write to register of the
                                                       FPGA
  exit/quit                                         -> disconnect from server
                                                       (tcp-server mode only)

Start as TCP/IP-Server:
Usage: trbcmd [-h] [-d] [-p portnumber] [-b] [-V] tcp
Options:
  -h     give this help
  -p     tcp port number (default: 55555)
  -b     run in the background as daemon
  -d     turn on debugging information (default: off)
  -V     version number
```

A.4.1 PASTTREC register write

To write a value to a PASTTREC register one has to set the PASTTREC_REG (0xd400) register with an appropriate PASTTREC command and then issue a transaction with PASTTREC_REG_EXEC (0xd411) register. This blocks any subsequent SPI access until the read-back register has been read.

```
trbcmd w 0x6500 0xd400 0xabcd0 # set the PASTTREC command (followed by '0')
trbcmd w 0x6500 0xd411 0x1 # issue a transaction
```

A.4.2 PASTTREC register read

To read a value from a PASTTREC register one has to set the PASTTREC_REG (0xd400) register with an appropriate PASTTREC command, then issue a transac-

tion with PASTTREC_REG_EXEC (0xd411) register and read the collected value from the PASTTREC_REG_READ (0xd412) register.

```
trbcmd w 0x6500 0xd400 0xabcd0 # set the PASTTREC command (followed by '0')
trbcmd w 0x6500 0xd411 0x1 # issue a transaction
trbcmd r 0x6500 0xd412 # get the register value
```

A.4.3 Mode switch

To switch between the PASTTREC register access and the DS1820 one has to toggle the mode register PASTTREC_TEMP_SW (0x0023) to 0x1 for DS1820 or 0x0 for PASTTREC and then issue at least 3 PASTTREC_CLOCK ticks. By default, when the system started the controller is in the PASTTREC mode.

```
trbcmd w 0x6500 0x23 0x1 # change the access mode to DS1820

trbcmd w 0x6500 0xd416 0x1 # set SCK to '1'
trbcmd w 0x6500 0xd416 0x0 # set SCK to '0'
... x3
```

A.4.4 DS1820 temperature read

The OneWire state machine periodically updates the temperature value that is stored in a regular register TEMP_VALUE (0x0008) on the FPGA, hence access is limited to a single read command

```
trbcmd r 0x6500 0x0008 # read PASTTREC FEB temperature(31:16)
```

A.4.5 DS1820 unique ID read

The OneWire state machine periodically updates the unique ID value that is stored in a regular register's TEMP_ID (0x000a - 0x000b) on the FPGA. The value has more than 32b, hence access is limited to two read commands

```
trbcmd r 0x6500 0x000a # read PASTTREC FEB unique ID(31:0)
trbcmd r 0x6500 0x000b # read PASTTREC FEB unique ID(63:32)
```

A.5 TRB platform

The TRB5sc is an endpoint board that contains a single FPGA device used for the digitization of input signals and requires a concentrator board, such as TRBv3 to operate. The board can be connected to a peripheral FPGA of TRBv3 configured as a hub with an optical fibre and therefore become integrated into a system of a larger scale. The FPGA in the TRB5sc for FT readout is configured with a Time-to-Digital Converter (TDC) to digitize signals from the PASTTREC FEBs. The confirmation of proper migration of the TDC between TRBv3 and TRB5sc is included in the A.6 section below and consists of a successful measurement of the Time-Over-Threshold feature of the straw detector.

A system composed of a TRBv3 board acting as a concentrator and a TRB5SC used for the PASTTREC FEBs interface has been constructed and successfully tested for the readout data transport and control and monitoring messages exchange.

The TRBv3 and TRB5sc schematics are available online at www.trb.gsi.de

The complete source code of all components is available in an online repository: git://jspc29.x-matter.uni-frankfurt.de/projects

A.6 Tests

All the above-described mechanisms have been tested on a setup presented in Figure A.2. The setup consisted of PASTTREC FEB boards connected to the straw detector (30 straws), an addon card prototype and a TRB5SC as a readout and control platform. The components of the readout were evaluated by performing a series of checks listed in Tab. A.6 below.

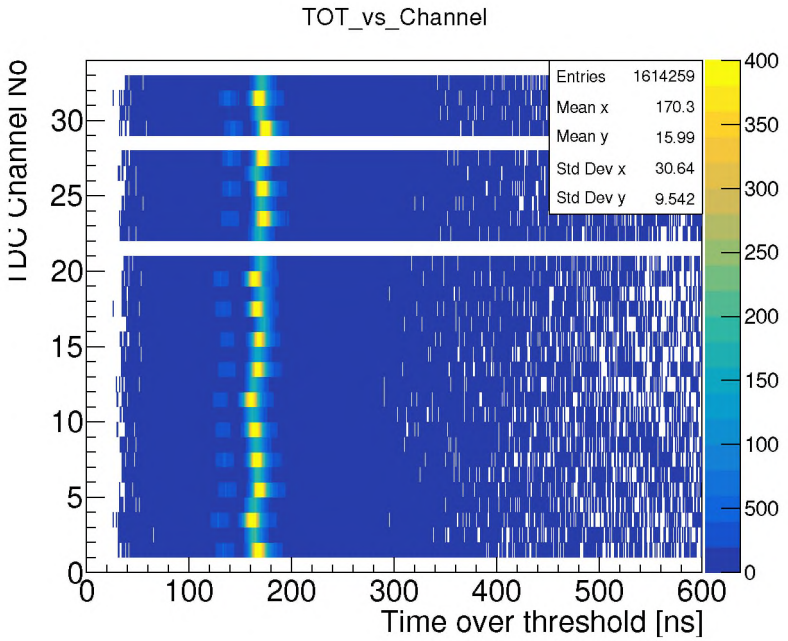


Figure A.4: TOT accumulated from illuminating 30 straws with ^{55}Fe radioactive source. Channel numbers 21 and 28 are missing data due to faulty straws.

After all the features and components in the readout test positive, the FEBs are connected to the straw modules for the tests of the full readout chain during the detector operation. The straw detector was illuminated with a radioactive source (^{55}Fe) and the data was gathered. The Time over Threshold (TOT) distribution was accumulated for 30 straws using the readout components described earlier. The TOT spectra obtained are shown in Figure A.4. The spread in the TOT among the channels confirms that all the PASTTREC channels have been properly configured with threshold and baseline settings. This presents the successful operation of the full readout chain for PANDA straws.

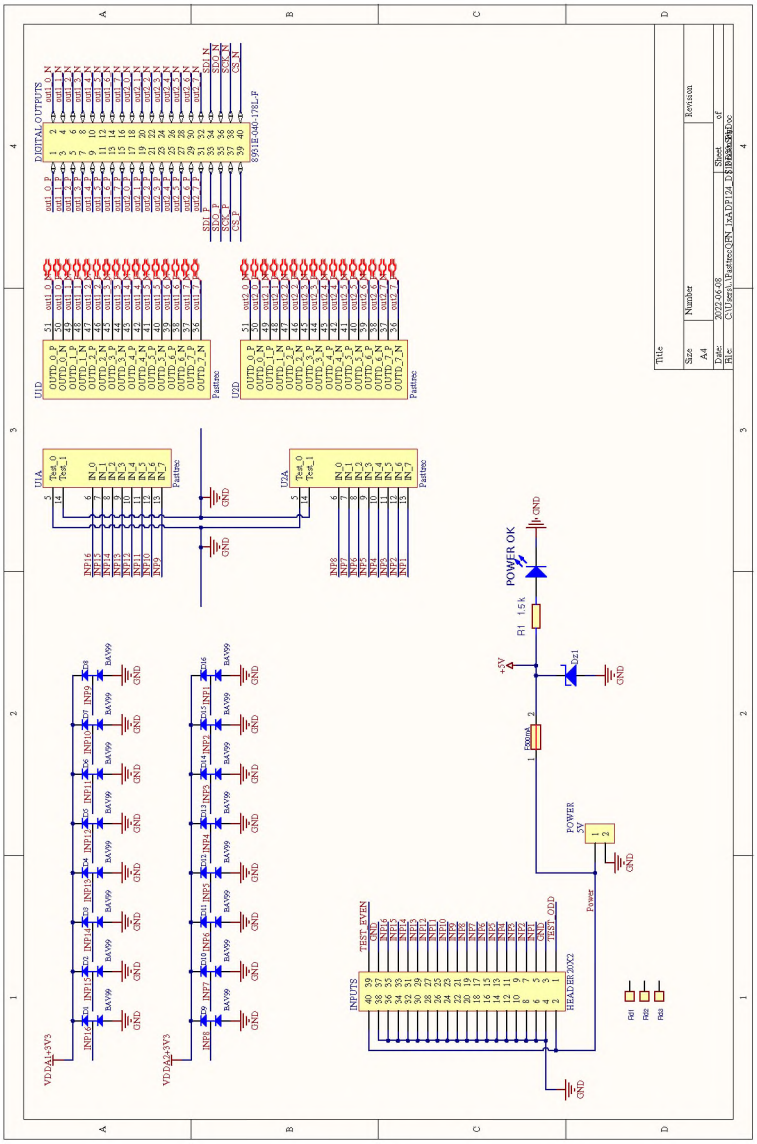
Table A.6: List of tested features

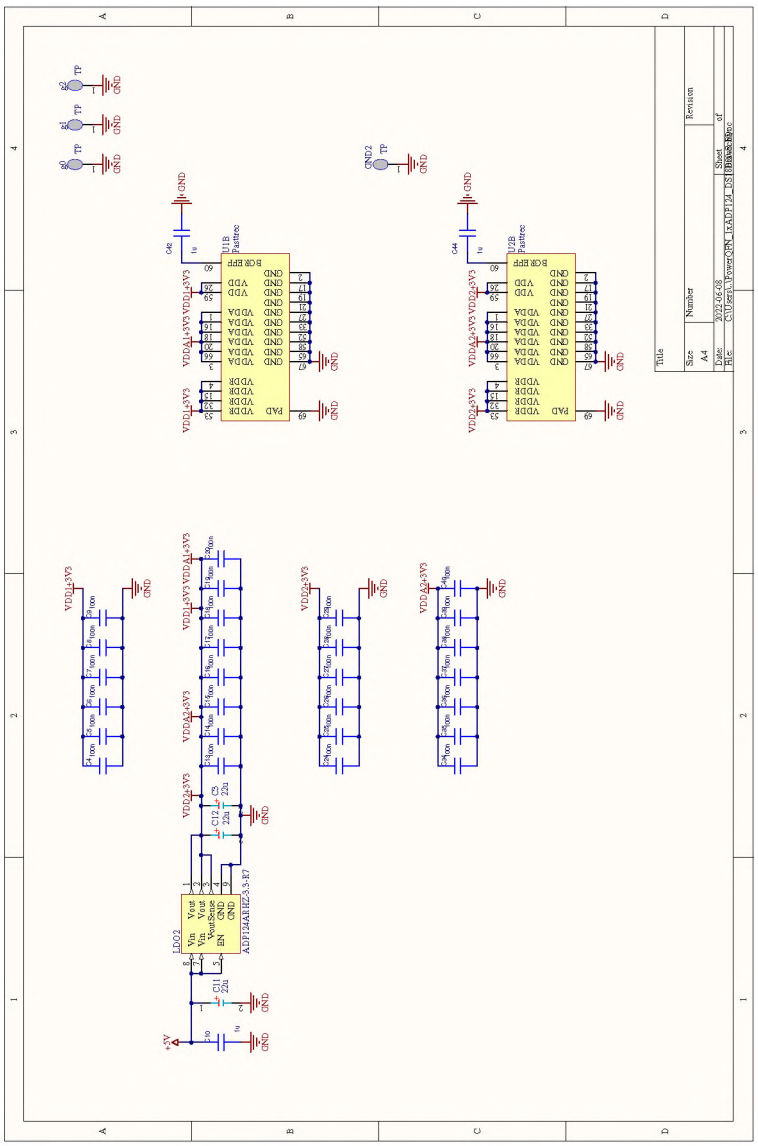
Tested feature	Description	Result
Hardware pin-out	Validation of the hardware connections on the add-on card between the TRB5SC and all 4 FEBs with an oscilloscope and multimeter	Positive
Firmware components compilation	Verify that modified and new firmware components are properly compiled and fit into the target FPGA device	Positive
PASTTREC addressing	Verify proper addressing of individual FEBs and PASTTREC chips	Positive
PASTTREC reset	Check proper reset procedure of all 4 FEBs by issuing reset sequence through TRB5SC	Positive
PASTTREC data lines	Check the mapping of the data and control lines running across different hardware, i.e, 4 PASTTREC FEBs, the add-on and the TRB5SC for digitization	Positive
Mode switch	Check the proper operation of the switching between connection to the PASTTREC or the DS1820 sensor	Positive
Temperature readout	Read and decode the temperature values from all 4 FEBs through TRB5SC	Positive
Unique ID readout	Read and decode the unique ID values from all 4 FEBs through TRB5SC	Positive
PASTTREC registers custom read and writes	Writes values to PASTTREC registers and confirms that configuration applied to ASIC is properly executed by read-back.	Positive
Stability of settings	Write value once and read-back values from PASTTREC registers after multiple 'mode switch' tests.	Positive
Cable length	Verify proper operation of the system with short and long (1 m and 10 m) cable lengths between the PASTTREC FEB and the add-on card	Positive

A.7 Schematics

A.7.1 PASTTREC FEB

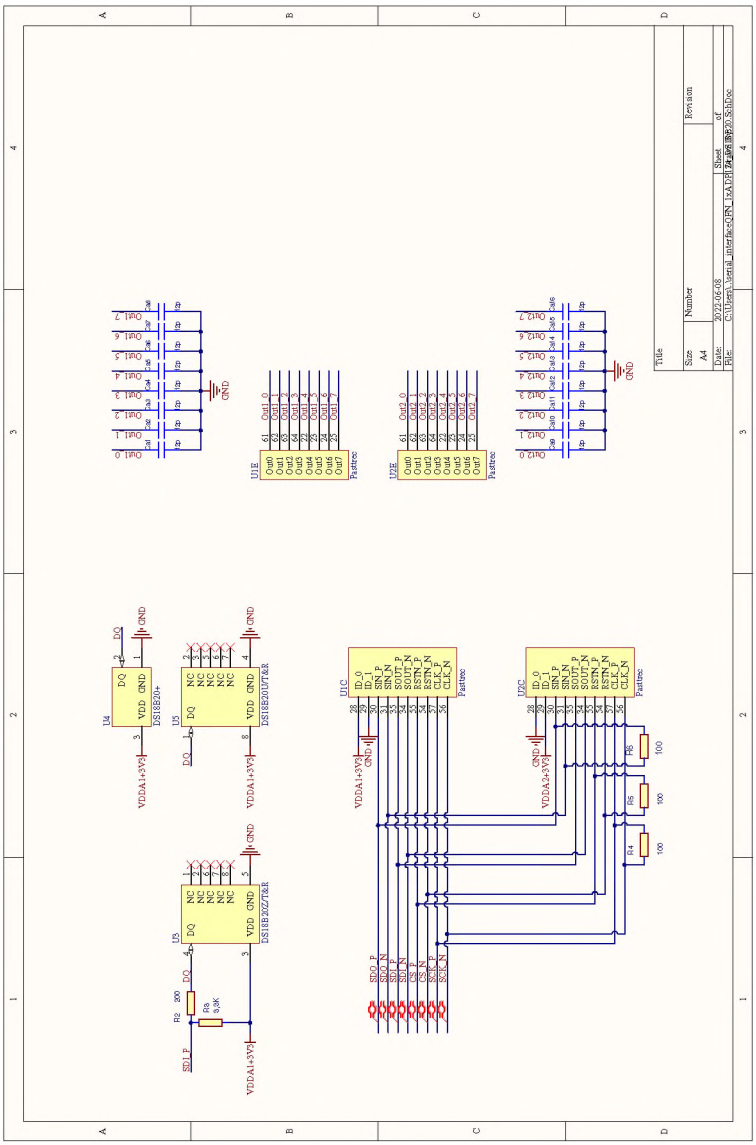
Design schematics of the PASTTREC FEB hardware PCB.

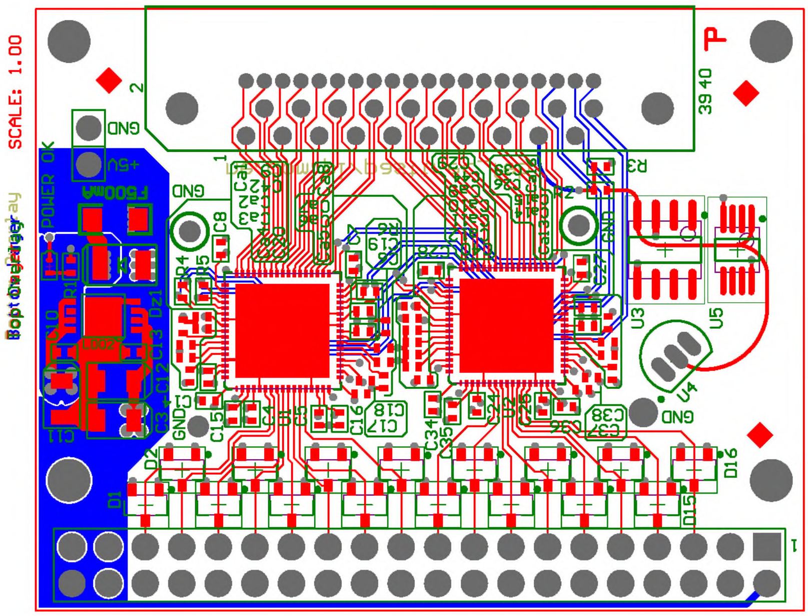


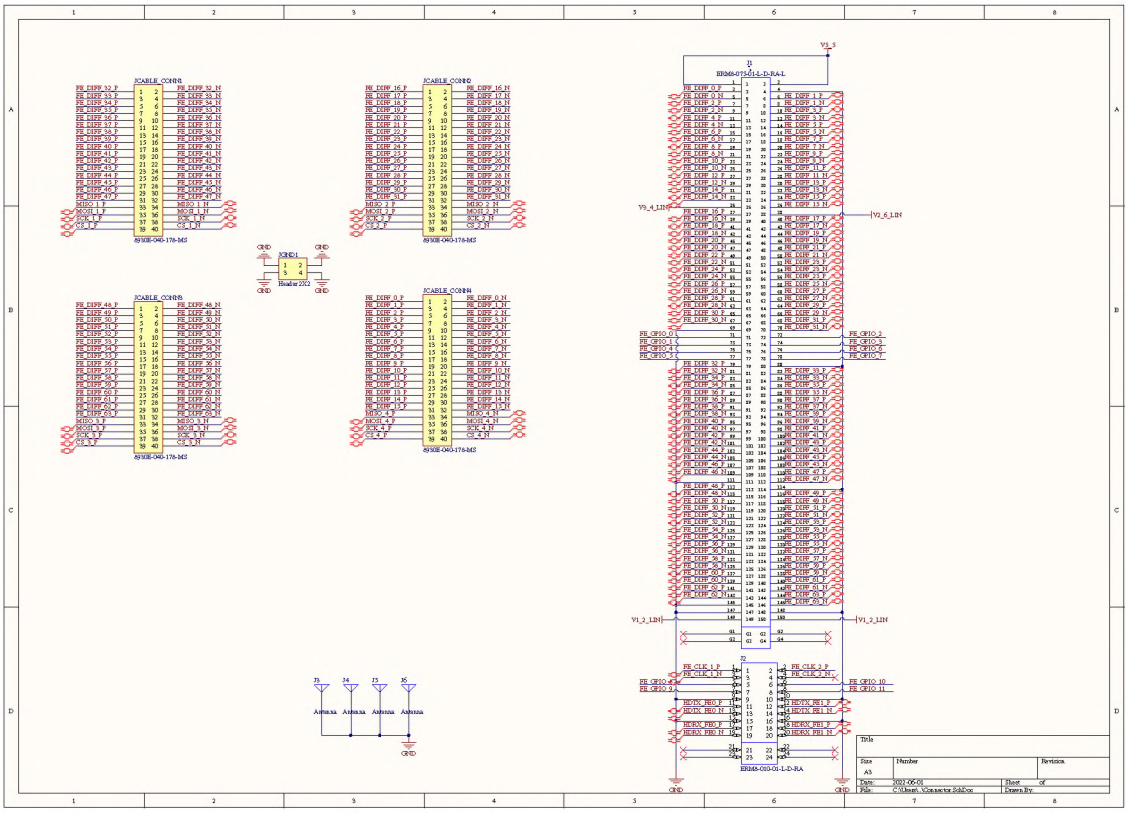


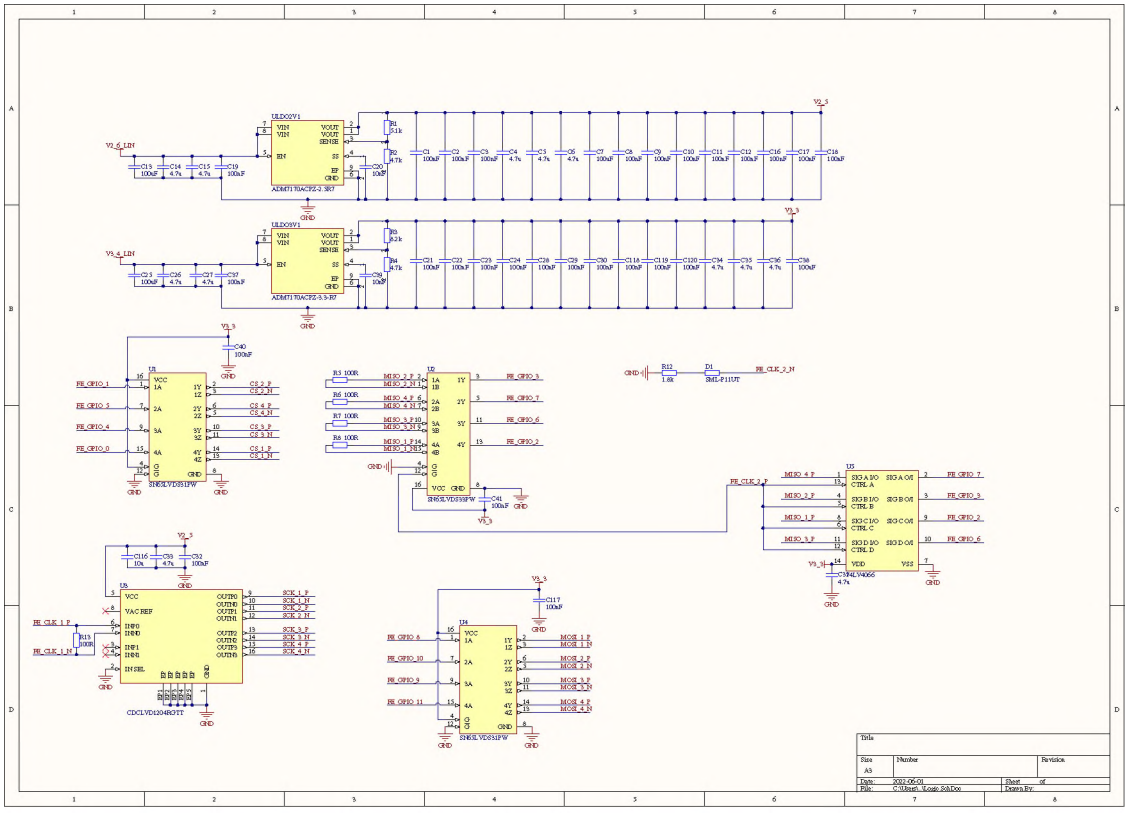
A.7.2 TRB5sc add-on

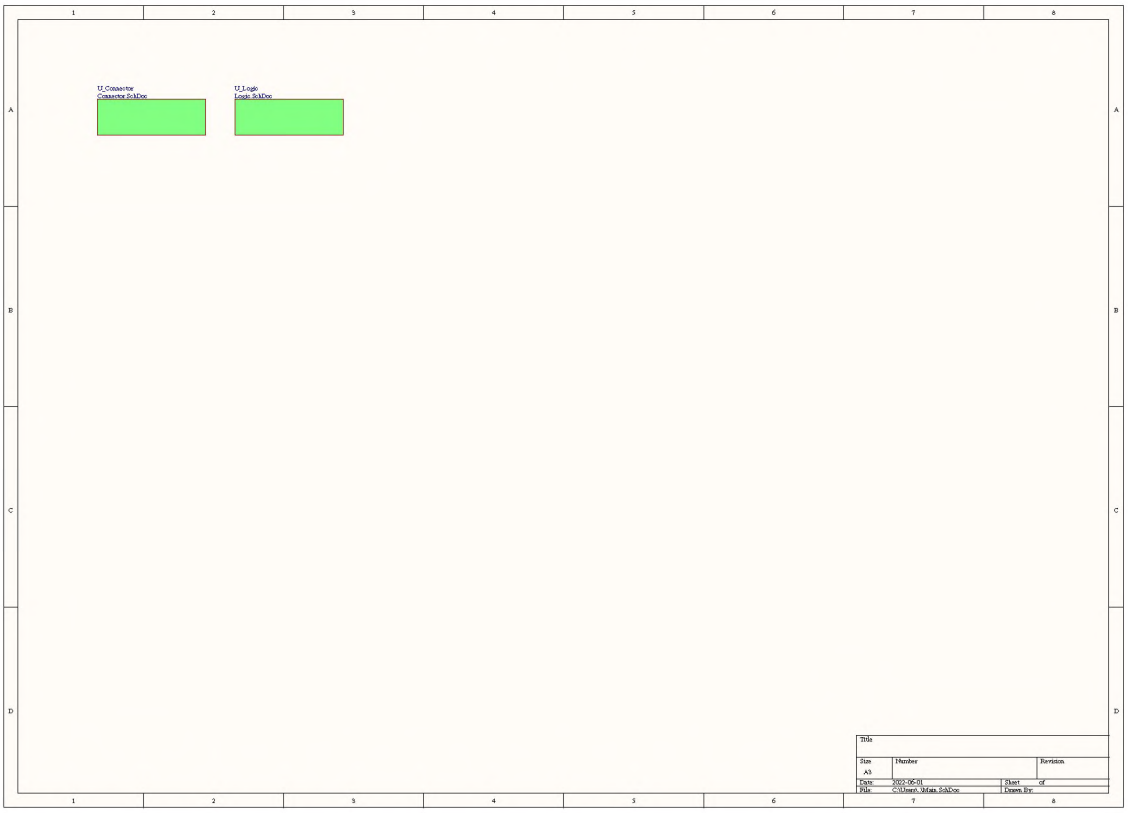
Design schematics of the PASTTREC - TRB5sc adapter card (add-on) after modification.

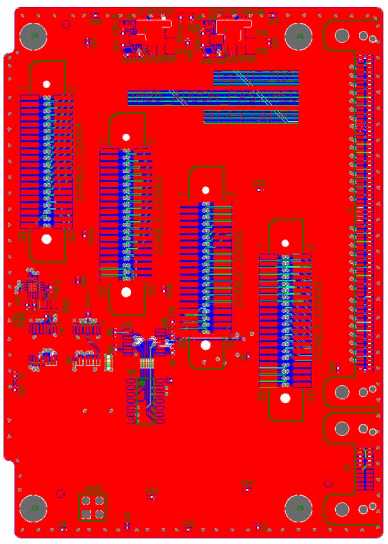












Jobname
TRB5SC_ADDON_4CONN

Date
10.2018

Designer
M.Traxler@gsi.de

Layouter
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Layer Nickname

Drd

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