Design, Construction and Prototyping of the Silicon Strip Tracker for the Micro Vertex Detector of the PANDA Experiment

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***Abstract*—The future PANDA-Experiment at the FAIR accelerator facility in Darmstadt/Germany utilizes an antiproton beam with momenta of 1.5 - 15 GeV/*c* incident on a hydrogen or heavy element fixed target. It addresses open questions concerning the strong interaction with one focus on high precision charmonium spectroscopy. The spatial and timing resolution in detecting fast-decaying particles e.g. in open-charm channels is crucial and requires the application of thin solid state detectors coupled with a fast untriggered readout electronics. The contribution will focus on the silicon microstrip tracker of the innermost subdetector, the Micro Vertex Detector (MVD), which is composed of double-sided silicon strip detectors (DSSDs). These are connected to ultra-thin flex modules carrying novel fast self-triggering front-end ASICs named PASTA. The construction of the DSSD modules, the carrier PCB and the architecture of the PASTA chip will be discussed as well as methods to qualify the sensors. An overview of the prototypes developed and tested up to now is given together with the future steps to be taken in order to arrive at the mass production of the full-scale modules.**

I. Introduction

STARTING from 2019, the Facility for Antiproton and Ion Research (FAIR) as an extension of the existing GSI research center in Darmstadt/Germany is going to host a set of experiments dedicated to the study of the strong interaction [1]. One of these is the PANDA detector (AntiProton Annihilations at Darmstadt), a full coverage precision spectrometer built around a fixed target with the beam antiprotons incident on hydrogen or heavier targets, whose main research focus will be rendered by high precision measurements of charmed channels with high statistics [2], [3]. In order to identify highly suppressed short-lived states such as open-charm decays, a vertexing and precise tracking is mandatory. This is accomplished with the Micro Vertex Detector (MVD) arranged closely around the interaction point in four barrel layers and several forward disks of highly granular semiconductor detectors (Fig. 1). While the two inner layers and inner forward disks comprise epitaxial hybrid pixel detectors, the outer barrels and outer forward discs are constructed of double-sided silicon strip detectors (DSSDs) to accomodate for the required spatial resolution [4]. The readout scheme of the MVD within PANDA is sketched in Fig. 2. The DSSD sensors are connected to front-end ASICs (named PASTA, see Sec. III) close to the sensitive components. Their digitized output data stream then is multiplexed and preprocessed through Module Data Concentrator (MDC) ASICs, which are placed close to the front-end electronics on the detector modules. This ASIC transmits the bundled data streams via differential electrical links to the outside of the detector where the transition to fast 3.2 GBit/s optical links via scalable GBT interface is achieved [5]. After a further multiplexing stage which additionaly couples the data stream and the whole readout chain to an experiment-wide locked phase synchronization via a receiver for the PANDA time distribution system (SODANET), optical links with up to 10 GBit/s bandwidth transmit the data to a farm of massively parallel compute nodes for event reordering, pattern recognition and event selection [6].

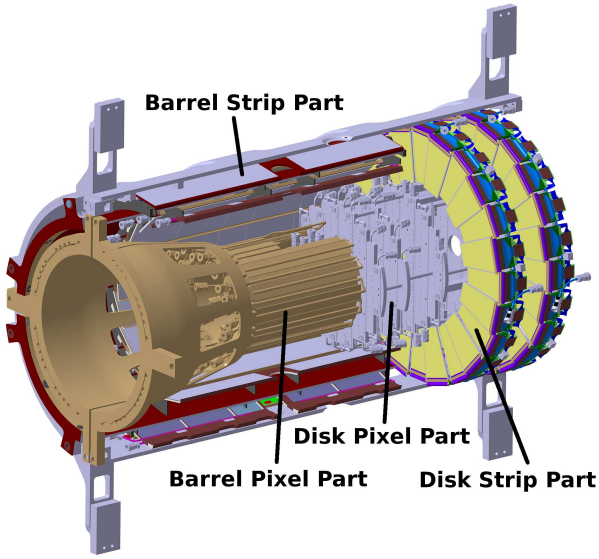

Fig. 1. CAD drawing of the PANDA Micro Vertex Detector.

II. Mechanical Construction

The silicon microstrip subdetector system of the MVD is composed of two parts different in construction and granularity for the two barrel layers and two forward disks, respectively. The barrels are organized in stave-ladder detector modules with 20 and 26 modules equipped for barrel layers three and

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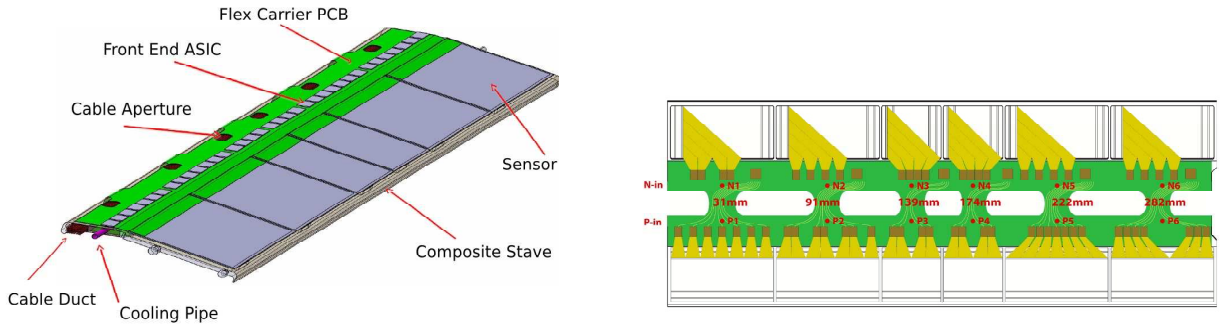

Fig. 3. CAD drawing of the proposed construction of one stave ladder of the silicon microstrip detector barrel (left). Geometric design of the thin-flex PCB hosting sensor interface structures, fan-out routing of all channels to the front-end electronics, front-end ASICs and multiplexing MDC ASICs. The PCB is bent around the stave ladder at the horizontal symmetry axis to accomodate for p- and n-side connections of the same sensors (right).

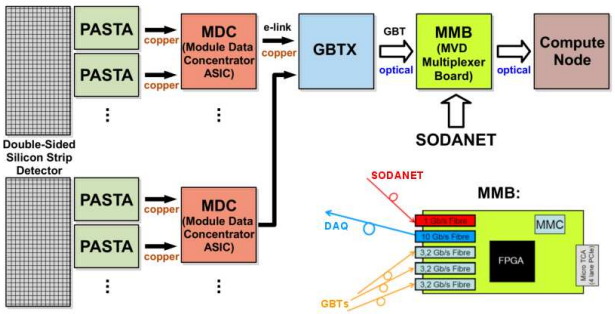

Fig. 2. Block schematic of the readout chain for the silicon strip tracker of the Micro Vertex Detector.

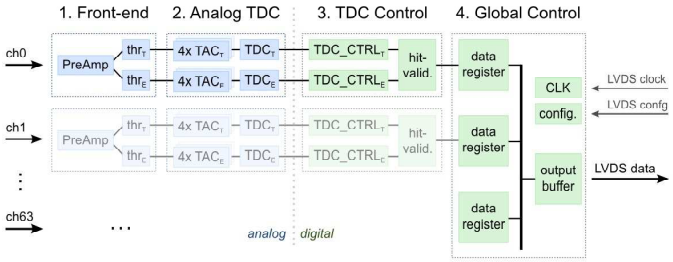

Fig. 4. Functional block schematic of the PASTA front-end ASIC.

four. Each detector module consists of a 2 mm thick ladder structure made of sandwiched carbon fiber reinforcements and embedded carbon foam and Rohacell fillings (Fig. 3 left) yielding very low material occupancy and therefore exhibit low small angle scattering of traversing particles. An embedded MP35N Nickel-Cobalt alloy cooling pipe (cooling medium is water) removes the heat from front-end electronic ASICs mounted on thin-flex PCB boards in thermal contact with the carbon carrier on top and bottom sides. For the routing of the required voltage supplies a cable duct has been foreseen which runs through the entire length of the module with apertures for cable drop-outs at regular intervals. The PCB carrying the front-end electronics and serving as an interface to the sensors with implemeted fan-in structures will be realized in thin-flex technology such that the material occupancy is kept very low and the flex PCB can be bent around the long side of the stave ladder to serve as bonding interface to p- and n-side sensor pads and host the front-end electronics of either readout side (Fig. 3 right).

III. Front-End Electronics

The readout of the DSSD sensors is accomplished with a customized fast self-triggering ASIC currently under development. This PANDA Strip Readout ASIC (PASTA) designated chip delivers time stamps and time-over-threshold (ToT) information with a time resolution of a few hundreds of picoseconds for every detector hit as digital data stream to the following data acquisition stage (Fig. 4). The PASTA front-end exhibits a channel multiplicity of 64 and the unique feature of a dual threshold time-to-digital-converter (TDC) block with an analog interpolating switched capacitor stage for the desired time resolution of fractions of the global 160 MHz clock period [7]. In order to suppress pile-up conditions, the output of each channel's preamplifier is cyclically distributed to up to four TDC stages. The power dissipation of this chip is considered a crucial design parameter due to the limited heat removal capacity within the Micro Vertex Detector and is estimated from simulations to 4 mW/ ch. A first full-size prototype of this ASIC is expected to be submitted in early 2015 in a commercial 110 nm CMOS process.

IV. Silicon Strip Sensors

The sensitive elements of the MVD strip tracker are comprised of double sided silicon strip detectors in p^+-n-n^+ configuration with p- and n-side pitches of 65 μm under a stereo angle of 90° for the rectangular barrel sensors and 45 μm under stereo angles of 15° for the trapezoidal forward disk sensors. The readout of the sensors is foreseen in every-other-strip configurations with one intermediate strip kept floating. A subset of the required total amount of 296 sensors was ordered from CiS GmbH in Erfurt/Germany and is scheduled for quality screening on delivery in 2015 covering screening of parameters such as capacitances, leakage current, biasing resistance and others for each sensor [8]. Other parameters like e.g. doping concentration and behavior under irradiation are monitored for wafer- and batch-wise subsamples only. One of the most important observables to be recorded is the sensor's backside capacitance in dependence of bias voltage

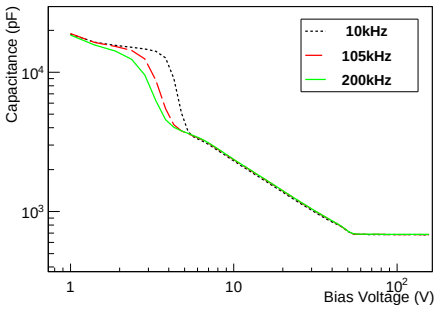

Fig. 5. Backside capacitance characteristics of a full size (6x3.5 cm^2) DSSD. The exponentially decreasing capacitance with increasing bias voltage implies regular depletion of the sensor volume. Transition towards a constant trend is due to exceeding the full depletion voltage of the sensor.

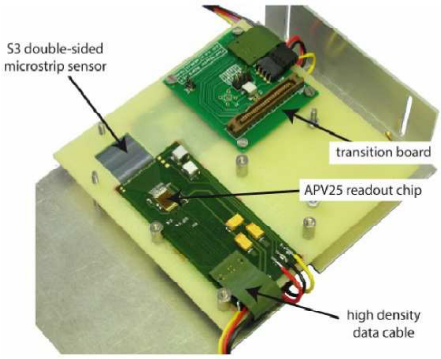

Fig. 6. Photograph of single-front-end flex prototype with implemented pitch adapting fan-out interface from connected sensor (type S3: 2x2 cm^2, 50 μm pitch, 90° stereo angle) and APV25-S1 front-end ASIC. The back side of the sensor is connected to an identical PCB flex not seen on this photograph. Connections from sensor to PCB and from PCB to the front-end ASIC are aluminum wire bonds. The ultra-thin PCBs are glued to a glass fiber support structure due to the fragility of the hybrid.

and test frequency (Fig. 5). Regular depletion behavior and full depletion voltage are inferred based on this data [9].

V. Prototyping

The feasibility of the construction of the module entities has been carefully scrutinized in several technological stages. The carbon ladder structure could be produced in a close-to-final prototype with embedded cooling pipe and cable duct. A thin-flex PCB was manufactured in a first version as single front-end prototype with the APV25-S1 [10] ASIC for the readout of a smaller DSSD, but featuring 65 μm strip pitch as in the final version (Fig. 6). This flex PCB and the succesful operation with a connected sensor marked the proof-of-concept for the usability of this technology yielding feature sizes as low as 50 μm. Both, interconnection to the 130 μm sensor structures on one side and fine-pitch fan-in routing towards the front-end ASIC interface were implemented and verified with this prototype. Results of first measurements yield the obtained signal-to-noise ratio vs. bias voltage and an energy loss spectrum as recorded during a beam test with 2.95 GeV/c protons (Fig. 7). The mechanical stability of the flex module proved to be of superior quality with no observed failure of wire-bonding connections even after several mount/unmount

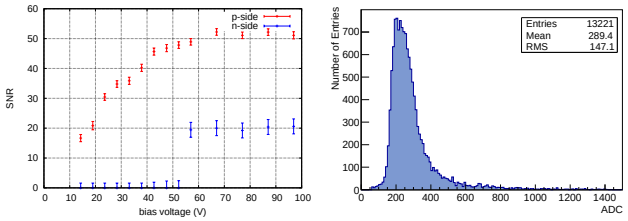

Fig. 7. Signal-to-noise ratio with respect to 1 MIP of p- and n-side obtained from bias voltage scan of flex prototype module (left). Energy loss spectrum measured during beam test with 2.95 GeV/c protons (right).

cycles and transportations to/from the beam test sites including inevitable shock and vibrational stress.

VI. Conclusion

The development of the silicon microstrip tracker for the PANDA experiment requires feasibility studies and prototyping with respect to mechanics, electronics, sensors and interconnection technologies. All these topics are being addressed with the construction of proof-of-concept and technological feasibility prototypes as shown above. Apart from the close-to-final full-size carbon stave ladder prototype and the start of the mass delivery of a part of the barrel DSSD sensors complying to the target specifications, the flex PCB hosting the readout structures of the barrel DSSD sensors progresses with technological prototypes developed to test handling and operation of a single front-end prototype including interconnection and small feature size challenges. The next step under development is the fabrication of a multi-front-end flex PCB to scrutinize large scale operation and system stability. Eventually, the close-to-final design of the flex PCB is going to utilize the PASTA front-end ASIC after it has been evaluated for stable operation.

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